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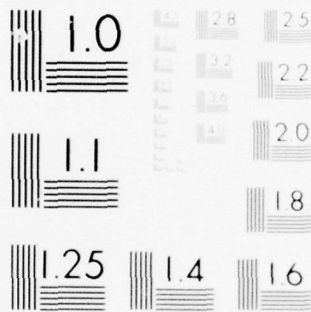
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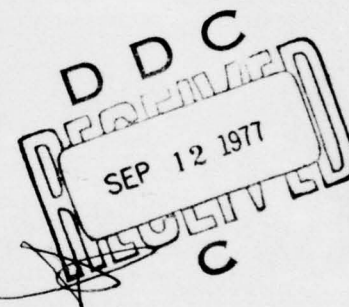
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Final Technical Report
August 1977

MULTIPLE CHIP SCR

RCA/Government Systems Division



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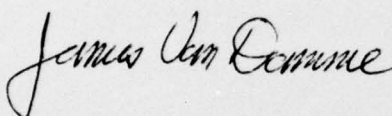
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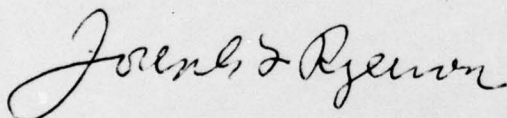
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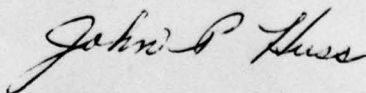
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19 REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER 18 RADC-TR-77-264	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) 6 MULTIPLE CHIP SCR	9	5. TYPE OF REPORT & PERIOD COVERED Final Technical Report, 12 Mar 76 - 31 May 77
7. AUTHOR(s) 10 R. Casolaro D. Pruitt	15	6. PERFORMING ORG. REPORT NUMBER 610 062 A1 8. CONTRACT OR GRANT NUMBER(s) F30602-76-C-0197
9. PERFORMING ORGANIZATION NAME AND ADDRESS RCA/Government Systems Division Missile & Surface Radar Moorestown NJ 08057	16	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62702F 45060365
11. CONTROLLING OFFICE NAME AND ADDRESS Rome Air Development Center (OCTP) Griffiss AFB NY 13441	11	12. REPORT DATE Aug 1977
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office) Same		13. NUMBER OF PAGES 98 12-45p.
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report) Same		
18. SUPPLEMENTARY NOTES RADC Project Engineer: James VanDamme (OCTP)		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Modulators, Pulse Thyristors Solid State Pulse Modulators Pulsers, Solid State Radar Thyristor Pulse Modulators Radar Modulators Hybrid Thyristor Switch		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This report presents the results of a program which proved the feasibility of utilizing SCR chips in hybrid circuit switches for use in high power radar modulators. Performance achieved was as follows: (cont'd)		

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Parameter	Liquid Colled Module	Series Air Cooled Switch
Peak Voltage	500	9,000 Volts
Peak Current	5,000	3,000 Amperes
Pulse Width	20	10 μ sec
Current Rise Time	2 $\frac{1}{2}$	1 μ sec
Repetition Rate	250	100 pps
Duty Cycle	0.005	0.001
Service	Continuous	Continuous

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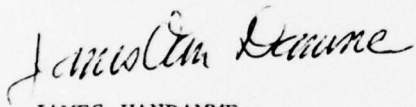
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EVALUATION

This program establishes the feasibility of developing a hybrid SCR module by combining series/parallel SCRs on a single beryllia substrate. The triggering circuits and voltage balancing circuits are also contained on the substrate. The modules are stacked in series to provide greater voltage holdoff.

An air-cooled 0.1% duty series switch ran successfully at 8.9 KV and 3000 amperes. A water cooled 0.5% duty single switch module switched 500 volts of 5000 amperes and showed promise for switching higher power pending solution of heat removal problems.

An SCR switch has a potential for low cost, significantly smaller size and weight, and greatly increased reliability relative to the thyratrons commonly used in radar modulators. The hybrid chip approach of this effort has additional advantages over packaged devices in that a switch can be made even smaller, lighter, and cheaper. Also, the isolation of the substrate allows significant circuit simplification and reduction in interconnections.



JAMES VANDAMME
Project Engineer

1.0 INTRODUCTION

This report contains the results of the Multiple Chip SCR Program conducted for the Rome Air Development Center under contract number F30602-76-C-0197. This program was performed by the RCA Missile and Surface Radar Division, Moorestown, New Jersey, during the period from 12 March 1976 to 31 May 1977.

This program established the feasibility of developing a Hybrid circuit SCR (Silicon Controlled Rectifier) module by combining a multiplicity of SCR Chips in a series/parallel configuration on a single ceramic substrate. The circuit for simultaneously triggering all of the SCR chips is included in the Hybrid circuit. A number of the modules are connected in series to provide greater voltage capability.

To meet the SOW requirements (Appendix A), a "10 chips in parallel" design was chosen. To obtain an optimum form factor, and to optimize trigger circuit design, two of these parallel groups were placed in series on a single 2.6" by 8" beryllia substrate. Thus, the RCA module design incorporates two RADC "Multiple Chip Packages" on one beryllia substrate.

Two of these modules were fitted with water jacket attachments for high duty cycle liquid cooled tests. Most were fitted with air cooling fins for use in a series air cooled switch. Ten air cooled modules were connected in series to produce a high voltage modulator switch.

The performance achieved during the test program was as follows:

<u>Parameter</u>	<u>Liquid Cooled Module</u>	<u>Air Cooled Series Stack (10 Modules in Series)</u>
Peak Voltage	500V	8.9 KV
Peak Current	5 KA	3 KA
Pulse Width	20 μ sec	10 μ sec
Rise Time	2-1/4 μ sec	1 μ sec
Duty Cycle	0.005	0.001

Some of these parameters were limited by available test set parameters: Particularly voltage and rise time for the liquid cooled module. The results achieved, particularly in the case of the series stack, are attractive for radar modulator applications.

2.0 BACKGROUND

The roots of the Multiple Chip SCR Program extend back to 1973, when RCA was engaged in a study of super power modulators (Reference 1). During this study, RCA became interested in the use of a multiplicity of small SCR's in series/parallel connection for a super power pulse switch. This interest was pursued, first in internal programs and then by contract (References 2 and 3).

The final outcome of these efforts was a successful switch module using 10 small packaged SCR's (2N3873) in parallel. The packaged SCR devices were mounted on a water cooled aluminum heat sink, and proved to be capable of conducting 6000 amperes peak with 20 microsecond pulses at 0.005 duty cycle. Twenty of these modules were stacked in series to provide a 10 KV (peak) switch (Reference 2), and thirty were stacked in series to provide a 15 KV switch (Reference 3).

During the latter portion of these efforts, a concept was developed for a Hybrid circuit SCR module. Advantages to be gained (over packaged devices) are:

- Significantly smaller in size and weight.
- Two parallel groups may be connected in series on one substrate, reducing interconnections. (See Section 4.2)
- Electrical isolation of SCR anodes from heat sink allows significant circuit simplification. (See Section 4.2)
- Potential low cost, competitive with thyratrons.

A proposal (in response to RADCR A-6-1039) for developing such a module (Reference 7) was supplied to the Rome Air Development Center, resulting in the Present contract: F30602-76-C-0197.

3.0 PROGRAM OBJECTIVES

3.1 SOW SUMMARY

The statement of work applicable to this program is reproduced in Appendix A to this report. A brief summary of the tasks and technical requirements is listed below:

1. Design, fabricate, and test of a multiple chip silicon controlled rectifier.
2. Investigation of Multiple Chip configurations in typical standard packages such as flat packs or "Hockey Puck" types and/or hybrid assemblies on beryllia substrates or other materials of equal thermal characteristics.
3. The number of individual chips to be mounted within the package selected shall be determined by physical size and electrical isolation limitations.
4. The distribution of trigger signals shall be integral within the package. DC isolation shall be provided when multiple packages are stacked in series for higher voltage operation.
5. The minimum chip size to be considered shall be in the 600V, 600 Ampere range.
6. The objective ratings for the multiple chip package shall be:
 - 600 Volts
 - 6000 Amperes
 - 0.005 Duty
 - 20 Microsecond Pulse
 - One Microsecond current Rise Time
7. Control of Rise and Fall Time so as to be no worse than that of a single device.
8. The design of the thermal dissipation system shall include any effect on package size and provide means for stacking packages to enable series operation at high voltage without susceptibility to corona, arcing, or serious current leakage through cooling system.
9. Deliver ten sample devices at end of contract.
10. Prepare Preliminary Hazard List.

3.2 SUMMARY OF ACCOMPLISHMENTS VERSUS THE OBJECTIVES

Table 3-1 summarizes the task descriptions and status, with a cross reference between SOW paragraphs and paragraphs of this report.

TABLE 3-1. SUMMARY OF ACCOMPLISHMENTS

SOW Task No.	Short Description	Status	Report Reference
4.1.1	Design, Fabricate, and Test	Complete	4, 6, and 7
4.1.2	Investigate Package Configuration	Complete	4.2
4.1.3	Selection of number of Chips per package	Complete	4.2
4.1.4	Trigger Distribution Design	Complete	4.2
4.1.5	Minimum Chip Size	Complete	4.1
4.1.6	Objective Ratings	Complete	7.1, 7.2
4.1.7	Rise and Fall Time Control	Complete	4.2
4.1.8	Thermal Design	Complete	5.
4.1.9	Sample Deliveries	*	
4.1.10	Preliminary Hazard List	Complete	Appendix C

*Will be delivered at end of contract (31 May)
in accordance with SOW requirement.

4.0 MODULE DESIGN

4.1 CHIP SELECTION

Paragraph 4.1.5 of the statement of work (Appendix A) required that the minimum chip size be in the 600 volt, 600 ampere range. Since this was considered to be near optimum for the rise times and pulse widths required, a specification was written for a 600 volt peak, 600 ampere peak chip. This specification is attached to this report as Appendix D. Other key chip specifications were:

- RMS Current Rating: 40 Amperes
- Current Pulse Rise Time: 1 Microsecond
- Recovery Time: 40 Microseconds Max.
- Off State dv/dt : 20 V/Microsecond, Min.
- Center Fired Gate
- "Shorted Gate" Design
- 0.20 inch Square Chip
- Glass Passivated Chip
- 95/5 Solder Coated Electrodes

The best chip offer was from Unitrode Corporation, Watertown, Massachusetts. Unitrode offered their SCR chip R044060 to satisfy the requirement. Following a trip to Unitrode to discuss the chip application, a quantity (500) of these chips were procured for this project.

4.2 CIRCUIT DESIGN

The circuit design was closely patterned after the previous successful design using packaged devices (See Figure 4-1).

The circuit of Figure 4-1 operates as follows: The 10 main SCR's, SCR2 through SCR11, are connected in parallel with the anodes connected to a common heat sink. The main SCR's are triggered simultaneously from a common gate bus, via gate current sharing resistors R2 to R11 and isolating diodes D3 to D12. The gate voltage is derived from the main anode to cathode voltage, which is stored on C1 and

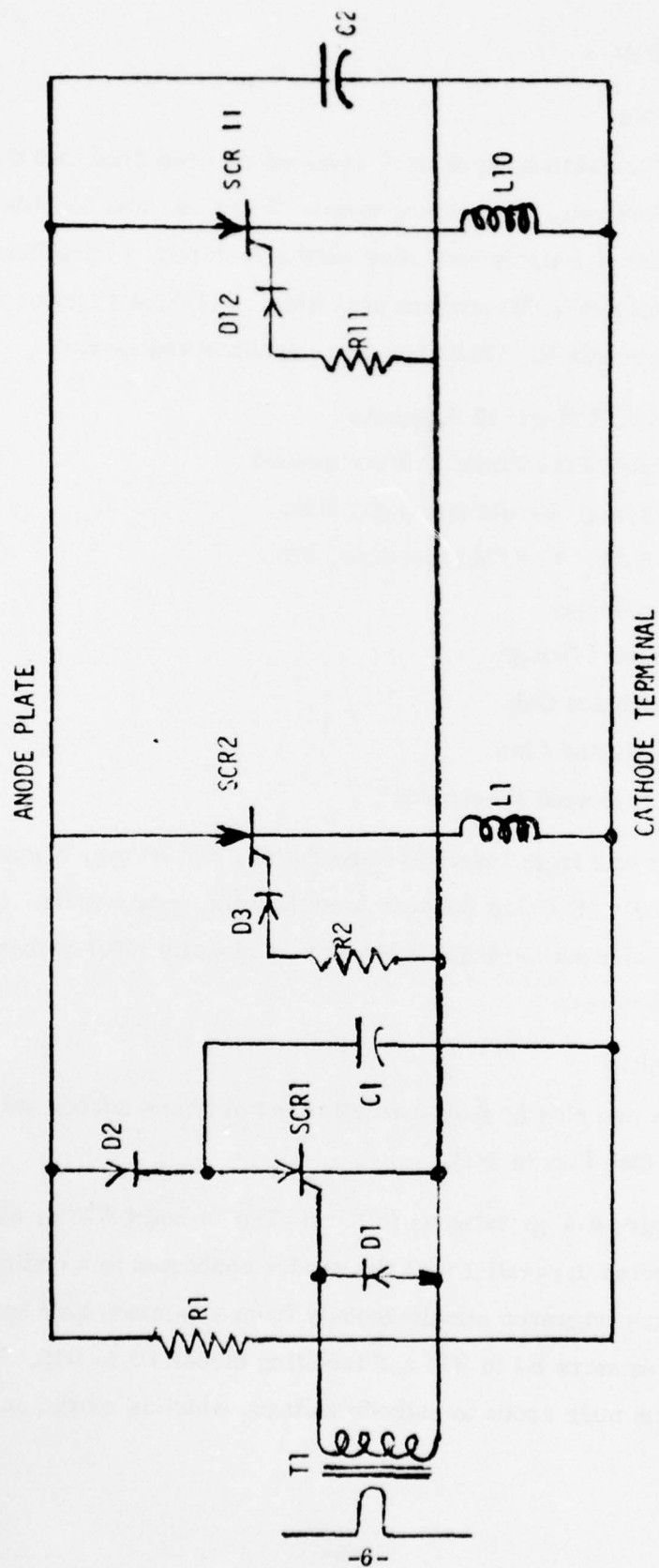


Figure 4-1. Parallel SCR Switch

transferred to the gate bus when the trigger SCR, SCR1, is triggered. SCR1's gate trigger comes from the secondary of pulse current transformer T1, a small ferrite toroid with a 50 turn secondary and a one turn primary. The primary turn is a high voltage insulated wire. The primary wire can be threaded through any number of module toroids, triggering all of these modules simultaneously when a 50 ampere current pulse is fed through the primary wire. Thus, series (and high voltage) operation is easily achieved with a simple trigger circuit.

With the hybrid chip circuit on an insulating beryllia substrate, some simplifications and improvements were possible:

- Testing with the packaged device circuits has shown that isolating diode D1 was not necessary, and that one capacitor (C1) was adequate for voltage division in a series string. Accordingly, D1 and C2 were eliminated.
- The Circuit fuses can be located in the anode leads, which are now electrically isolated from each other. This in turn allows the elimination of gate isolating diodes D3 through D12, which had previously been required to prevent the gate circuit being shorted to the anode bus through a failed SCR.
- The same type of SCR chip is used for the pilot SCR as for the main SCR's. Although overrated for the application, it will simplify the manufacturing process and enhance reliability.
- Because of the smaller size of the chips, it is convenient to place two circuits similar to Figure 4-1 in series on a single substrate. This results in a better form factor when stacking modules in series.

Figure 4-2 is a schematic diagram of the resulting SCR multichip module. The module contains 22 SCR chips: 10 in parallel by 2 in series plus 2 trigger (or pilot) chips. As pointed out earlier in Section 1.0, this module contains two RADC "Multiple Chip" packages.

4.3 CIRCUIT LAYOUT

Trial layouts were made by hand to determine optimum physical layout and substrate size. The information was then transferred to the applicon automatic drafting system to generate complete layout information and printed circuit screen information. The resulting drawings comprise sheets 1 through 17 of RCA drawing number HS12577-1 (Appendix F of this report).

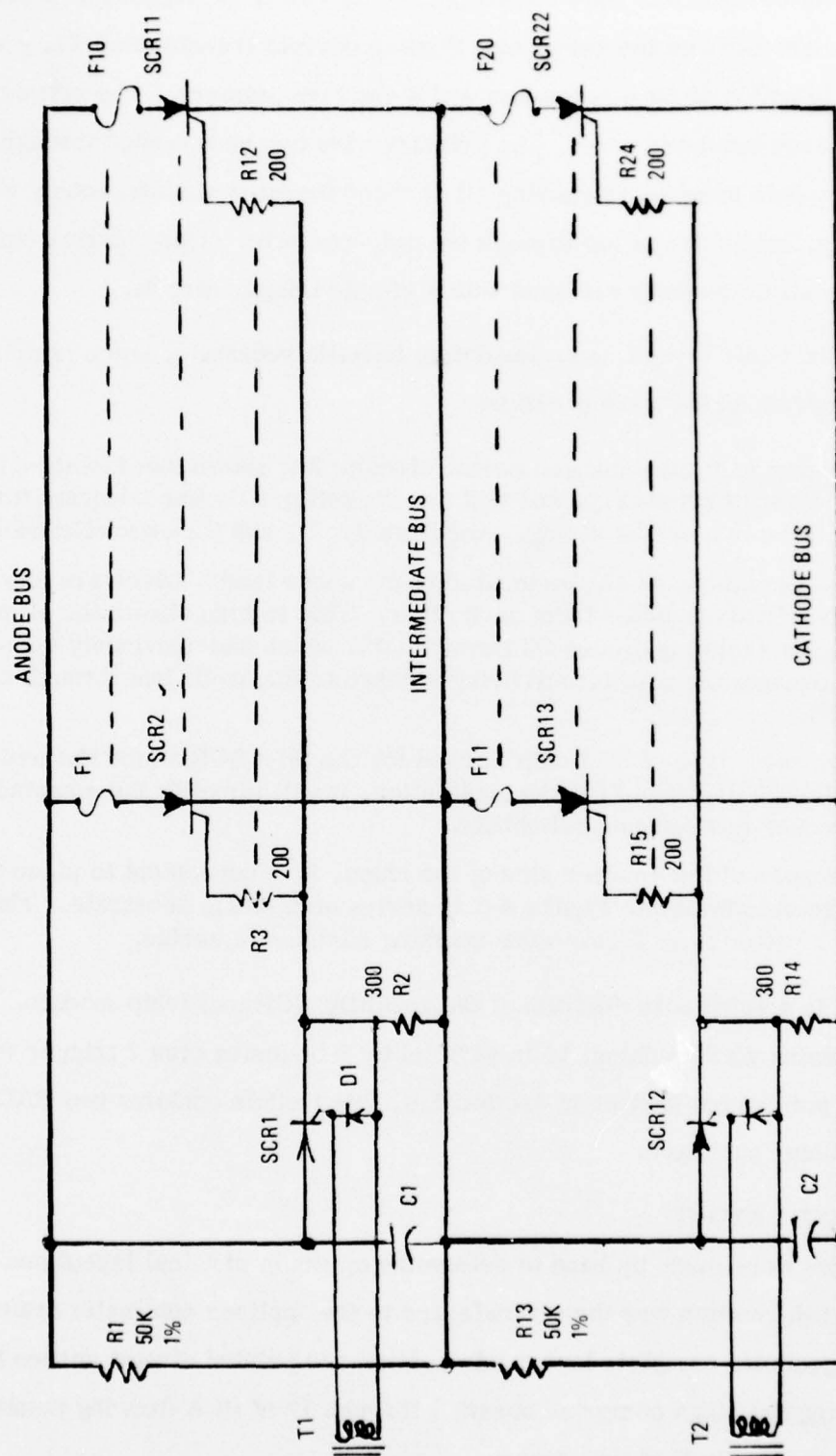


Figure 4-2. Multiple Chip SCR Schematic

The composite layout is also shown in Figure 4-3. Callouts shown in Figure 4-3 are identified as follows:

1. Beryllia Substrate
2. SCR Chip Anode Contact
3. SCR Chip Cathode Contact
4. SCR Chip Cathode Contact
5. Gate Bus
6. Anode Terminal (1 of 5)
7. Cathode Terminal (1 of 5)
8. Gate Connection (1 of 22)
9. Intermediate Bus
10. SCR Chip
11. Toroidal Trigger Transformer (1 of 2)
12. Capacitor (1 of 2)

4.4 HYBRID CIRCUIT DESIGN

After finalizing the circuit layout, a sketch and specification was prepared for the Beryllia Substrate. A copy of the substrate specification is attached to this report as Appendix E. These substrates were supplied by Ceradyne, Inc., under a competitive procurement.

From the Applicon drawings (Appendix F), screen drawings were generated. These screens, procured from a local firm, were used to print the thick film hybrid circuits on the beryllia substrates:

- Conductor Metallization
- Resistor Patterns
- Dielectric Patterns

The hybrid circuit processing procedure (simplified) is as follows:

- Screen, dry and fire conductor pattern on substrate
- Screen and dry first resistor pattern
- Screen and dry second resistor pattern

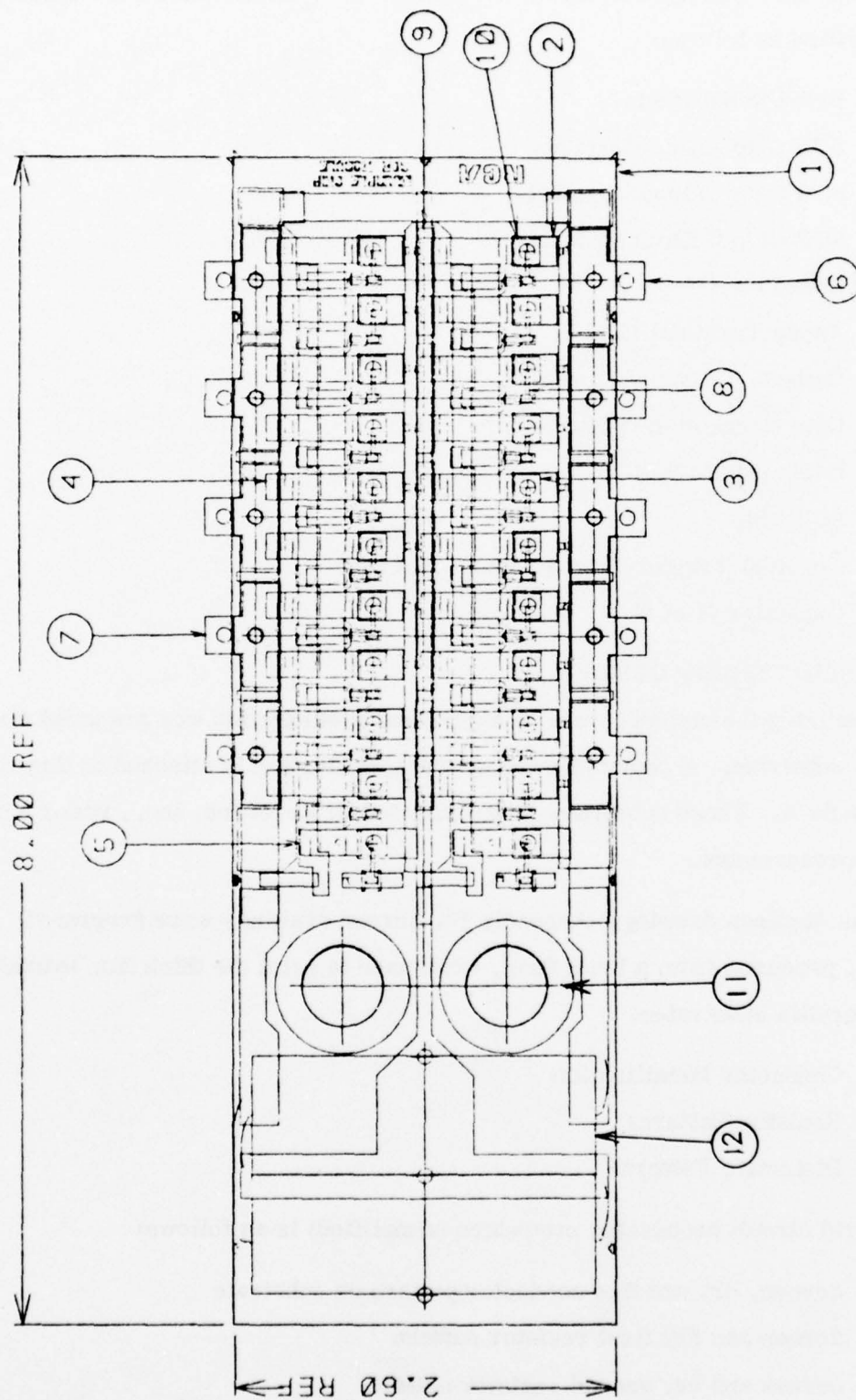


Figure 4-3. Multichip SCR Module Layout

- Fire Resistors
- Screen, dry, and fire insulator pattern
- Trim Resistors
- Attach connector pads to BeO substrate with 95-5 solder
- Attach anode and cathode pads to SCR chips with 95-5 solder
- Test and categorize SCR chips
- Attach SCR assemblies, gate leads, and miscellaneous components to BeO substrate (with 63-37 solder reflow)
- Apply silicone dielectric coating to SCR chips
- Preliminary module test
- Attach cooling fins to module (epoxy)
- Final module test.

5.0 THERMAL ANALYSIS

5.1 SCR CHIP POWER DISSIPATION

For short pulses (10 to 20 microseconds), the device voltage drop during the pulse is not constant: Several microseconds are required to reach minimum drop. From observations and measurements made on both packaged devices and chips over the past several years, the following conclusions were reached:

- (a) For the chip size under consideration, and for peak currents of hundreds of amperes, the resistive component of voltage drop dominates the semiconductor junction drop, i. e., the devices are nearly linear in the high peak current region.
- (b) The average value of voltage drop over a 20 microsecond pulse, with 600 amperes peak current, is about 12 volts for this size device, when properly triggered.
- (c) The device on state resistance is highly sensitive to gate trigger current: Higher gate trigger current gives lower on state resistance.
- (d) Variation in on state resistance among typical devices ranges up to about $\pm 20\%$.

The range of applications envisioned for the multichip SCR module is from 3,000 amperes peak at 0.001 duty to 6,000 amperes peak at 0.005 duty. In terms of the individual chip, the range is from 300 amperes peak at 0.001 duty to 600 amperes peak at 0.005 duty, which is a range of 20:1 in device dissipation: from 1.8 watts average to 36 watts average per chip.

This range of dissipations is to be demonstrated by an operation at each extreme: An air cooled operation at the lower dissipation and a liquid cooled operation at the higher dissipation. Table 5-1 shows the parameters to be demonstrated:

TABLE 5-1. SWITCH OPERATING PARAMETERS

Parameter	Forced Air Cooled	Forced Liquid Cooled
Pulse Width	10 μ sec.	20 μ sec.
Repetition Rate	100 pps	250 pps
Duty Cycle	0.001	0.005
No. of Modules	10 in series	1
Peak Voltage	10 kV	600 Volts
Peak Current	3 KA	6 KA
Peak Power	15 MW	1.8 MW
Average Power	15 kW	9 kW
Average Module Dissipation	36 Watts	720 Watts
Average SCR Dissipation	1.8 Watts	36 Watts
SCR Dissipation/ Pulse	0.018 joules	0.144 joules

For the analysis presented in sections 5.2 and 5.3 following, it is assumed that the average module dissipation is 750 watts in the forced liquid cooled case, or 37.5 watts in the air cooled case. (This assumption amounts to an "upward" rounding off of the 720 watt calculated figure to 750 watts.)

5.2 CHIP TRANSIENT TEMPERATURE RISE

During the pulse, it may be assumed that little (or none) of the dissipated energy will leave the SCR chip. This slightly pessimistic assumption will yield a "worst case" value for the chip transient temperature rise during the pulse.

Figure 5-1 is a cross section of the SCR chip geometry. For the transient analysis, it was assumed that the dissipated power would be dissipated in equal amounts at each of the three semiconductor junctions. This is, once again, a pessimistic assumption since much, if not most, of the power will be dissipated in the bulk silicon as an I^2R loss.

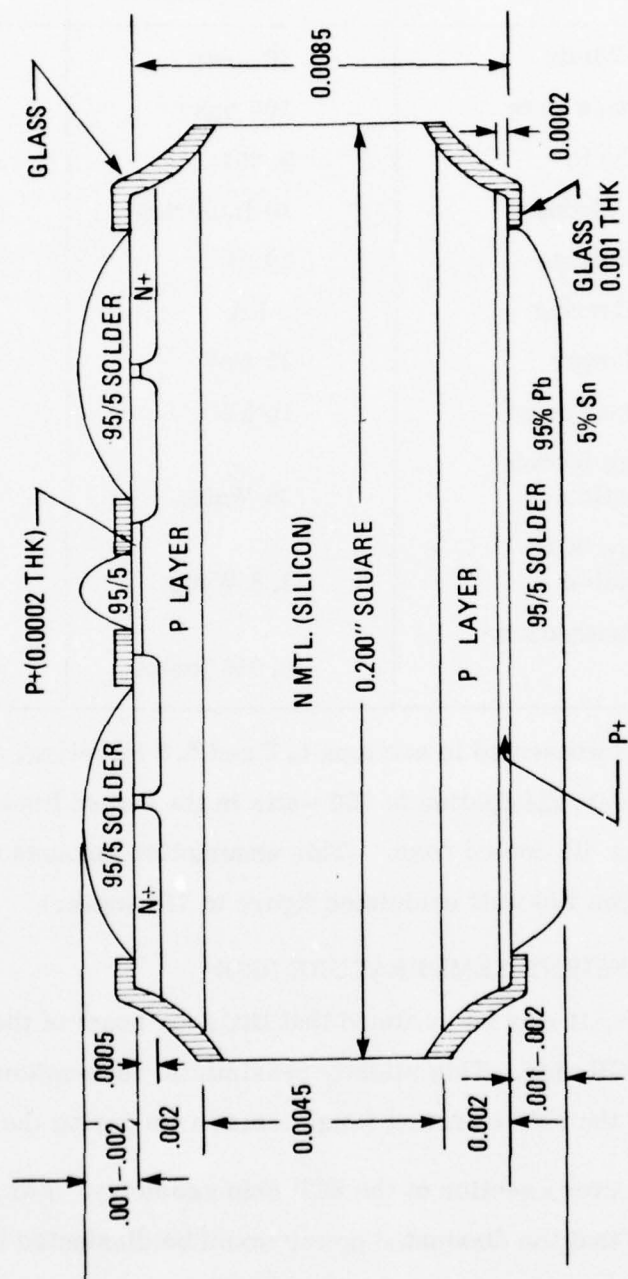


Figure 5-1. Chip Cross Section

Figure 5-2 is a cross section diagram showing the simplified chip geometry used in the analysis. The chip power dissipation (7500 watts peak for the high power case; 3750 watts peak for the lower power case) was assumed to be divided equally among the three semiconductor junctions, as indicated by "Q1", "Q2", and "Q3" of Figure 5-2.

The transient temperature rise was analyzed on a Hewlett Packard Model HP9830 calculator, using a stepped analysis with 1/2 microsecond steps. Using chip dimensions as given in Figure 5-2, and utilizing handbook constants for the specific heat and thermal conductivity of silicon and solder, the appropriate equations were derived as follows:

(a) For the lower power case:

Peak Current = 3,000 amperes

Peak Dissipation = 3,750 watts

Pulse Width = 10 microseconds

$$T_6' = 0.98461104 T_6 + 0.01538896 T_7 + 0.614957$$

$$T_7' = 0.01295057 T_6 + 0.97193867 T_7 + 0.015109945 T_8 + 0.517549$$

$$T_8' = 0.0201466 T_7 + 0.94819447 T_8 + 0.03165894 T_0$$

$$T_0' = 0.0118721 T_8 + 0.98642449 T_0 + 0.0017034 T_9 + 0.2587747$$

In these equations:

- The temperatures (T's) are in degrees fahrenheit above the starting temperature
- T' denotes temperature 1/2 microsecond after the previous calculation.

(b) For the high power case:

Peak Current = 6,000 amperes

Peak Power = 7,500 watts

Pulse Width = 20 microseconds

$$T_6' = 0.98461104 T_6 + 0.01538896 T_7 + 1.2299$$

$$T_7' = 0.01295057 T_6 + 0.97193867 T_7 + 0.015109945 T_8 + 1.035098$$

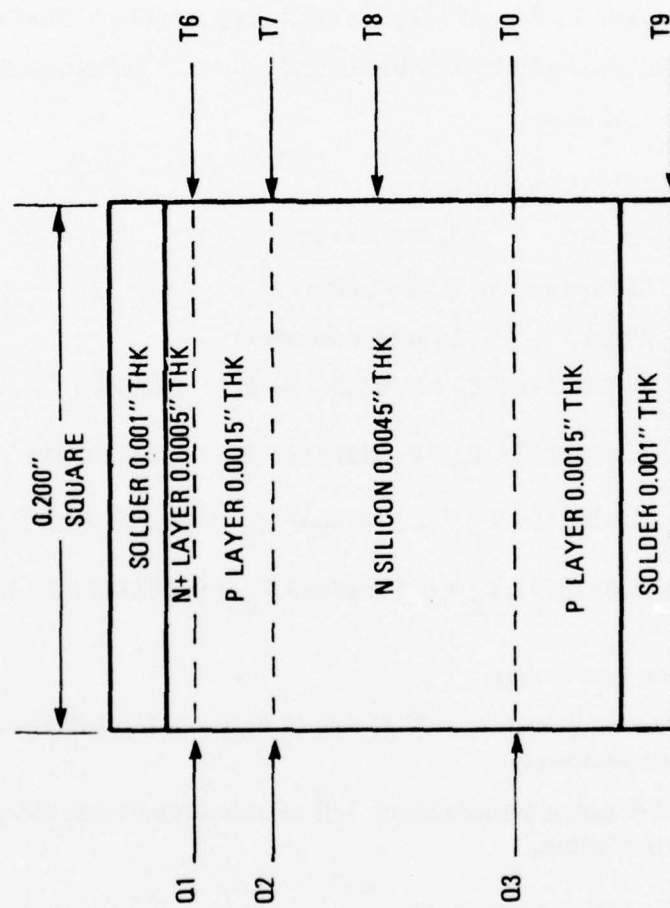


Figure 5-2. Simplified Chip Geometry

$$T_8' = 0.0201466 T_7 + 0.94819447 T_8 + 0.03165894 T_0$$

$$T_0' = 0.0118721 T_8 + 0.98642449 T_0 + 0.0017034 T_9 + 0.5175494$$

Where the definitions are the same as for the lower power case.

The calculated junction temperatures were printed for 1/2 microsecond increments, as shown in Table 5-2 for the low power case (3,000 ampere/10 microseconds) and in Table 5-3 for the high power case (6,000 ampere/20 microseconds). The largest transient junction temperature rise is calculated to be 26.4°C (47.45°F) at the end of the high power 20 microsecond pulse.

It is concluded that temperature rise during the pulse is not serious over the intended range of operations.

5.3 STEADY STATE TEMPERATURE RISE

The temperature rise from the semiconductor junction to the substrate surface may be calculated using thermal conductivities. Thermal path resistances are calculated from these material conductivities and the path geometry.

The chip manufacturer (Unitrode) indicates that the thermal resistance from chip junction to chip surface is approximately 0.6°C/watt. Other items in the thermal path are:

- A Copper Pad
(4 watts/SQCM/°C/CM)
- A Solder Interface
(0.4 watts/SQCM/°C/CM)
- The BeO Substrate
(3 watts/SQCM/°C/CM)

TABLE 5-2. TRANSIENT CHIP TEMPERATURE RISE
(LOW POWER CASE)

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T5	T6	T7	T8	T9	0
0	0.14957	0.525513044	0.010587301	0.239947911	0
1	1.22853755	1.044385684	0.039309316	0.517753061	0
2	1.840600645	1.557059399	0.085033842	0.773643911	0
3	2.451253317	2.063945225	0.146702844	1.027833136	0
4	3.060250048	2.565425832	0.223327541	1.280518673	0
5	3.667592218	3.061857447	0.313903821	1.531884703	0
6	4.273227590	3.553571666	0.417807955	1.78210256	0
7	4.877109833	4.040877127	0.533992606	2.031331592	0
8	5.479198082	4.524061077	0.661783090	2.27971995	0
9	6.079456517	5.003390840	0.800473897	2.527405342	0
10	6.677853985	5.47911517	0.949405438	2.774515719	0
11	7.274363641	5.951465531	1.107961009	3.021169928	0
12	7.868962615	6.420657274	1.275563953	3.267478319	0
13	8.461631702	6.886890746	1.451675019	3.513543309	0
14	9.052355077	7.350352320	1.63578989	3.759459909	0
15	9.641120024	7.811215353	1.827436875	4.00531622	0
16	10.22791669	8.269641083	2.026174756	4.251193893	0
17	10.81273787	8.725779463	2.231590780	4.497168554	0
18	11.39557825	9.17976994	2.443298779	4.743310214	0
19	11.97643676	9.631742180	2.660937422	4.989683636	0
20	12.55531135	10.08181674	2.884168572	5.236348691	0

↳ 10 use

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TABLE 5-3. TRANSIENT CHIP TEMPERATURE RISE
(HIGH POWER CASE)

--- HIGH POWER CYCLE ---					
	T6	T7	T8	T9	T10
0	1.2299	1.051025902	0.851174595	0.513995753	0
1	2.457047314	2.020770832	0.876619518	1.02550605	
2					
3	3.681279922	3.11411774	0.170067647	1.54728768	
4					
5	4.902451986	4.127868714	0.297405613	2.055666038	
6					
7	6.120432164	5.150849094	0.44654957	2.561037000	
8					
9	7.335103510	6.123711340	0.627907435	3.063768924	
10					
11	8.546361444	7.107138669	0.835615605	3.564204482	
12					
13	9.754113302	8.081749338	1.067904783	4.062662367	
14					
15	10.95827734	9.046114860	1.3225656	4.559438886	
16					
17	12.15879193	10.00677288	1.600947036	5.05430945	
18					
19	13.35556475	10.95821992	1.896809939	5.549029965	
20					
21	14.5485721	11.90291891	2.215920589	6.042338124	
22					
23	15.73775825	12.84130056	2.551126422	6.534954628	
24					
25	16.92388478	13.77376556	2.903348247	7.027084309	
26					
27	18.10452004	14.70060667	3.271577647	7.518917192	
28					
29	19.28283898	15.62241060	3.654371239	8.010629478	
30					
31	20.45562071	16.53925983	4.052346587	8.502384466	
32					
33	21.62525199	17.45153427	4.463178184	8.994333412	
34					
35	22.79092282	18.35951283	4.886593696	9.486616336	
36					
37	23.95262882	19.26345483	5.321870456	9.979362766	
38					
39	25.11036653	20.16368140	5.768332196	10.47269244	
40					
41	26.26414036	21.0601767	6.225345987	10.96671597	
42					
43	27.41395736	21.95338914	6.69251939	11.46153543	
44					
45	28.55982489	22.84343245	7.168697796	11.95724494	
46					
47	29.70175556	23.73048663	7.65361930	12.45393121	
48					
49	30.83976394	24.61471988	8.147625536	12.95167403	
50					
51	31.97386697	25.4962853	8.649233309	13.45054669	
52					
53	33.10408373	26.37532982	9.158358769	13.9506165	
54					
55	34.2304352	27.25198692	9.67460137	14.45194513	
56					
57	35.35294414	28.12638140	10.19758774	14.95458599	
58					
59	36.47163486	28.99862918	10.72696652	15.45859962	
60					
61	37.58653307	29.86803798	11.26240874	15.96402359	
62					
63	38.69766577	30.73710786	11.80360593	16.47090481	
64					
65	39.80506106	31.6035318	12.35026902	16.97928085	
66					
67	40.90874006	32.46819616	12.90212658	17.48918715	
68					
69	42.00875674	33.33118116	13.45892418	18.00065533	
70					
71	43.10511788	34.19256134	14.020423	18.51371377	
72					
73	44.1978629	35.05240593	14.58639691	19.02836789	
74					
75	45.28702383	35.91077925	15.15664143	19.5447003	
76					
77	46.37263318	36.76774106	15.7309531	20.06267102	
78					
79	47.45472388	37.62334692	16.30914816	20.58231764	

C 20 use

The following table summarizes the calculated thermal resistances from the chip junction(s) to the surface of the B_eO substrate:

Path Material	Resistivity, $^{\circ}C/Watt$
Chip (Silicon)	0.6
Copper Pad	0.04
Solder Junction	0.05
B_eO Substrate	0.16
Total	0.85

Using the above value for thermal resistance, the total temperature rise from substrate surface to the chip junction may be calculated for the two primary operating conditions:

Condition	Dissipation/Chip	ΔT
I. Low Power	3.75 watts	$3.2^{\circ}C$
II. High Power	37.5 watts	$32^{\circ}C$

The final cooling medium will be forced air in Case I (low power), and liquid in Case II (high power).

Two additional factors must be kept in mind:

- The transient (during the pulse) temperature rise, calculated in Section 5-2, must be added to the steady state rise to obtain the peak temperature rise.
- The maximum allowable junction temperature is $125^{\circ}C$.

From these additional factors, the maximum permissible substrate (B_eO) temperature is calculated to be:

- For Case I (low power): $114.8^{\circ}C$
- For Case II (high power): $66.6^{\circ}C$

The final step in solution of the cooling problem is to supply adequate air flow (Case I) or liquid flow (Case II) to maintain the B_eO surface at or below the indicated temperatures.

The peak dissipated power flow, through the B_eO surface immediately opposite the SCR chip, is approximately 5 watts/sq. cm. for the low power case and approximately 50 watts/sq. cm. for the high power case.

For the high power case, direct cooling of the B_eO with a forced liquid flow, using water or a fluorocarbon, can hold the B_eO temperature to approximately $20^{\circ}C$ above the coolant temperature. Thus, a forced liquid coolant at $40^{\circ}C$ (max.) can hold the B_eO substrate temperature below the $66^{\circ}C$ maximum allowed.

For the low power case, forced air cooling is appropriate. With the aid of copper fins cemented to the substrate, an air flow of 600 linear feet per minute, past the fins, holds the substrate temperature rise to approximately $35^{\circ}C$ above ambient (experimental result).

Thus, for the low power case, an ambient air temperature up to $65^{\circ}C$ is permissible with the indicated air flow.

A Rotron "TARZAN" fan, supplying 270 CFM air flow at 0.2 inches of water static pressure, supplies 650 feet/minute over the 59 square inch intake area of the 10 KV series switch stack.

5.4 CONCLUSIONS

The above analysis indicates that the Hybrid Multichip SCR modules should perform as required without excessive temperature rise.

In fact, as documented in sections 7 and 8 of this report, the objective peak current rating of 6 KA at 20 μ second pulse width and 0.005 duty cycle could not be achieved on a sustained basis. The problem must be thermal in nature, since 6 KA peak at 20 μ second pulse width was readily achieved at lower duty cycles.

In searching for a reason (or reasons) for this discrepancy, the following possible reasons have been identified:

- The value used for voltage drop (average over the pulse) may be in error by as much as 2:1, i.e., as much as 20 to 25 volts rather than the 12 volts used in the analysis. This parameter is very difficult to measure because of inductive effects and the pulse environment.
- The final stage of heat removal may be inadequate. Heavier fins, soldered (rather than epoxied) might give more efficient heat removal in a forced liquid bath.

Refer to Section 9 of this report (conclusions) and Section 10 (recommended future programs) for additional discussion.

6.0 SWITCH CONSTRUCTION

6.1 CHIP PROCESSING

The SCR chips are received from the vendor (Unitrode) in a 49 chip plastic carrier as shown in Figure 6-1. The chip electrodes have been pre-tinned with 95-5 lead tin solder. Before any meaningful high current tests can be made, anode and cathode contacts must be soldered to the chips. Ten chips are shown in Figure 6-1 with anode and cathode electrodes attached. The cathode electrodes have circular holes provided to permit access to the gate electrode with either a test probe, or eventually with a soldered gate contact. The first chips were assembled with straight, flat cathode electrodes. However, the thermal expansion stresses set up during final module assembly resulted in cracked chips. To solve this problem, thermal expansion loops were provided in each cathode electrode (2 loops per cathode electrode) as seen in Figure 6-1.

After electrode assembly, the individual chips were tested to 600 amperes peak in the test fixture shown in Figure 6-2. Figure 6-3 is a schematic diagram of the chip test fixture. At 600 volts peak on capacitor C1, the circuit provides a half-sine wave shaped current pulse to the SCR under test (SCRUT), 600 amperes peak and approximately 10 microseconds across the base. Test repetition rate is approximately 3 pulses per second. (The low PRF precluded damage to the poorly cooled chip, which might result from a higher PRF.) The SCR voltage drop is monitored at J2 by observing on an oscilloscope alternately with the current pulse. The voltage drop is measured at the peak of the current pulse, and recorded. Typical voltage drops observed were 24 to 26 volts, with a few units showing as little as 20 volts or as much as 30 volts. The tested chips were categorized in increments of one volt and set aside for final assembly.

6.2 HYBRID CIRCUIT CONSTRUCTION

The printed circuit portion of the hybrid circuit is screened onto the 8 inch by 2.6 inch by 0.1 inch thick beryllia substrate as outlined in Section 4.4 (first 5 steps). Figure 6-4 shows the circuit after the printing, drying, and firing process is completed.

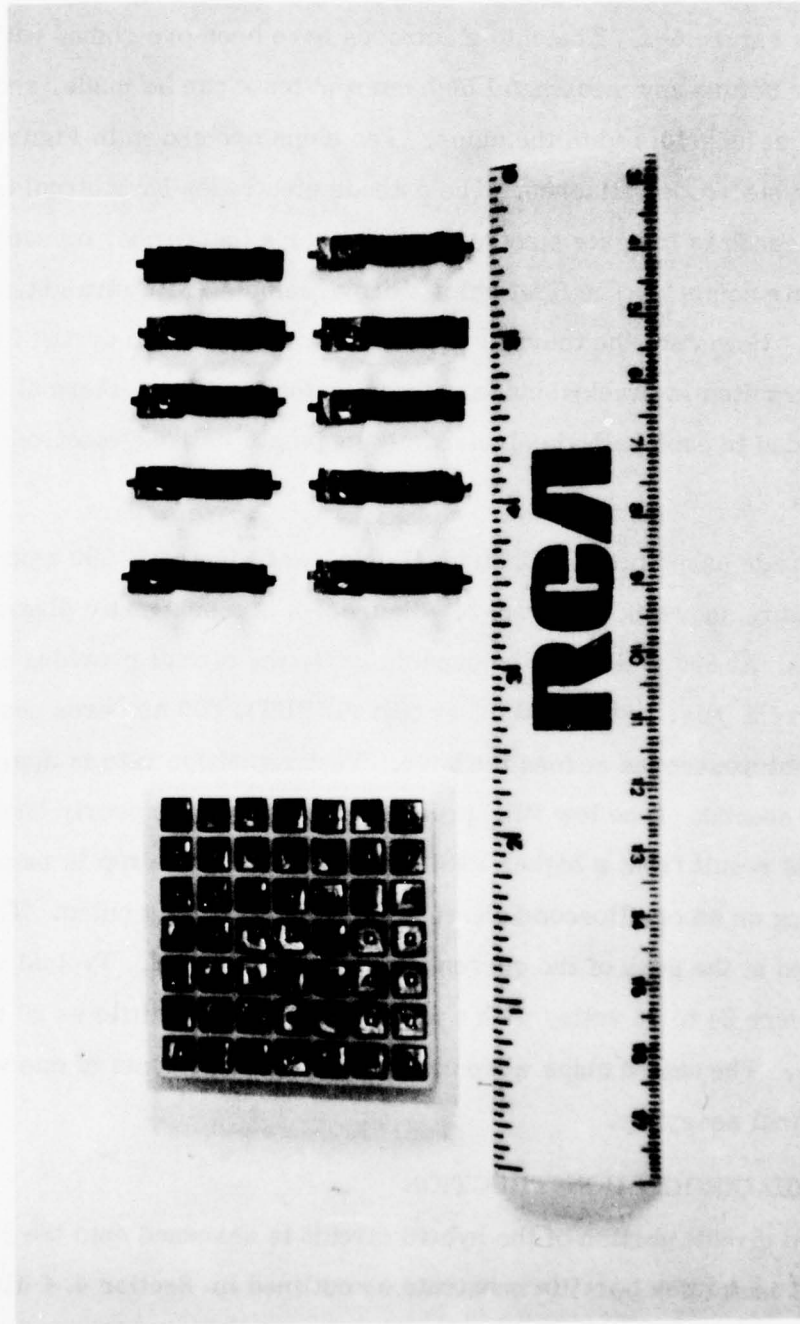


Figure 6-1. SCR Chips

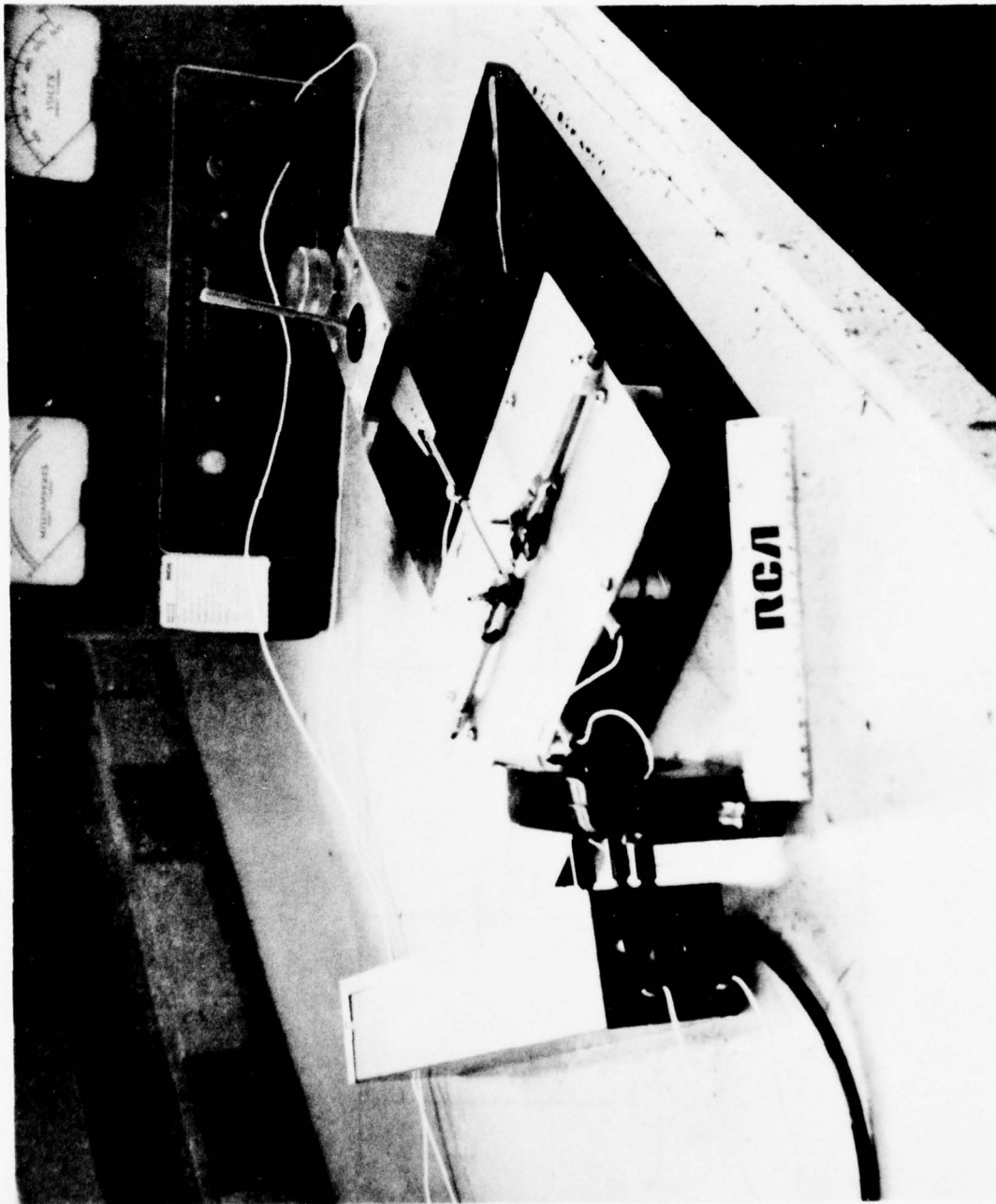


Figure 6-2. SCR Chip Test Set

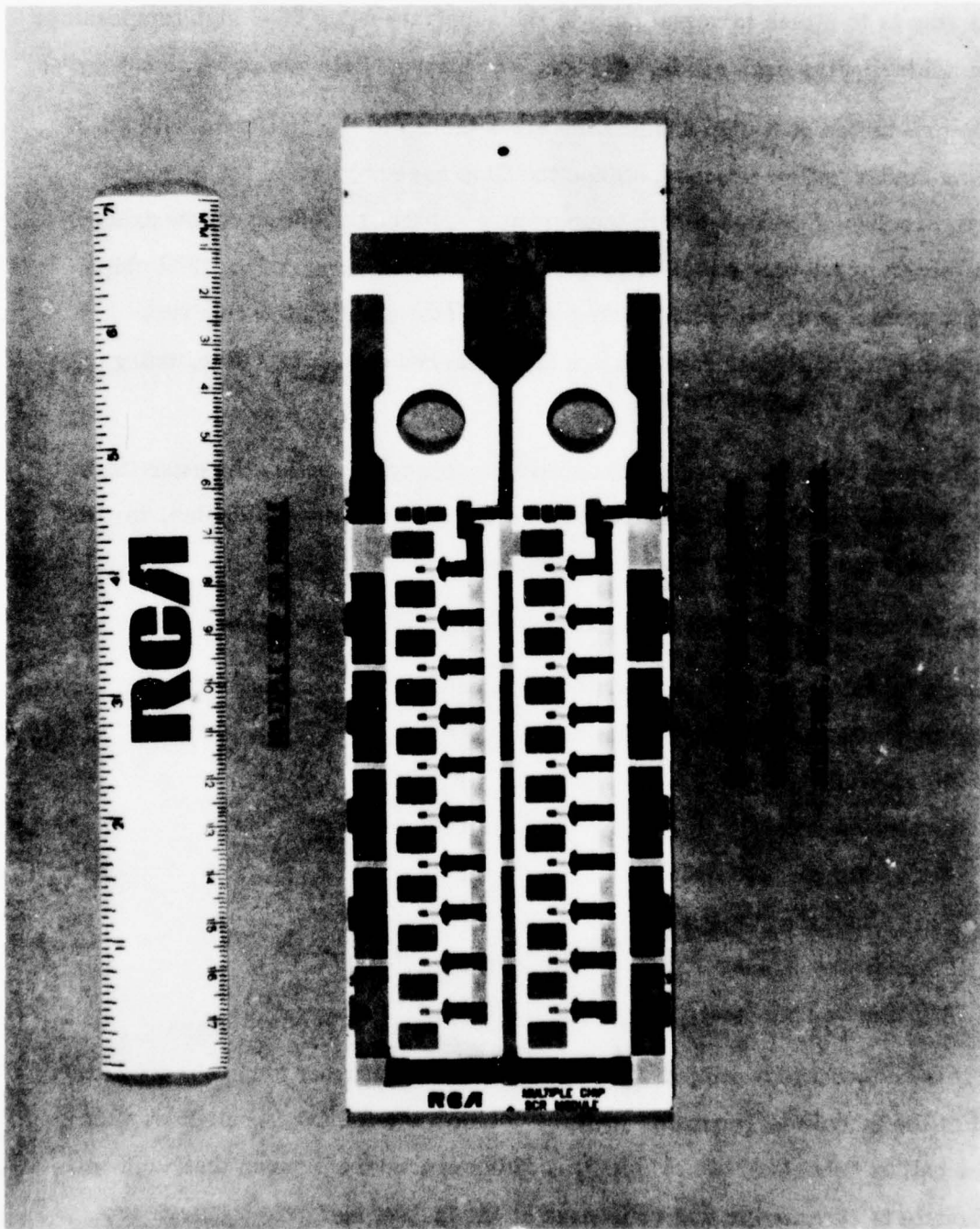


Figure 6-4. Substrate with Metallization, Dielectric and Resistor Layers

Next, the resistors are trimmed to $\pm 1\%$ of the desired value using an abrasion process.

The next step is to attach terminal pads to the substrate using 95-5 high temperature lead-tin solder: Five each anode, cathode, and intermediate bus pads.

Next, the pre-tested SCR chip assemblies are attached to the substrate with 63-37 solder in a solder reflow process. Since the Chip assemblies and the terminal pads were processed with 95-5 high temperature solder, the 63-37 reflow process does not loosen previously attached parts. Each parallel group of ten SCR chips is selected from a common voltage category, as determined in the chip test (Section 6.1). The SCR Gate contacts are also attached during this step, using 63-37 solder.

Finally, the trigger toroids are attached using an epoxy adhesive, the capacitors are attached with lacing cord, and the final electrical connections (diodes, toroids, and capacitors) made using a large soldering iron.

Figure 6-5 is a photo of a completed module, ready for electrical test.

To weed out initial defects, each module is subjected to a severe preliminary screening test with conditions as follows:

- Pulse Width: 14 μ sec.
- Repetition Rate: 50 pps
- Peak Voltage: 600 Volts
- Peak Current: 6 KA
- Duty Cycle: 0.0007
- Air Blast on Substrate

Each half of the module is subjected to this test for 30 minutes (one hour total) i. e., one half of the module is "shorted" with a 470 ohm resistor for 30 minutes, then the other half is "shorted" for 30 minutes. This procedure insures that each half of the module is stressed to 600 volts peak at the instant that gate triggers are applied.

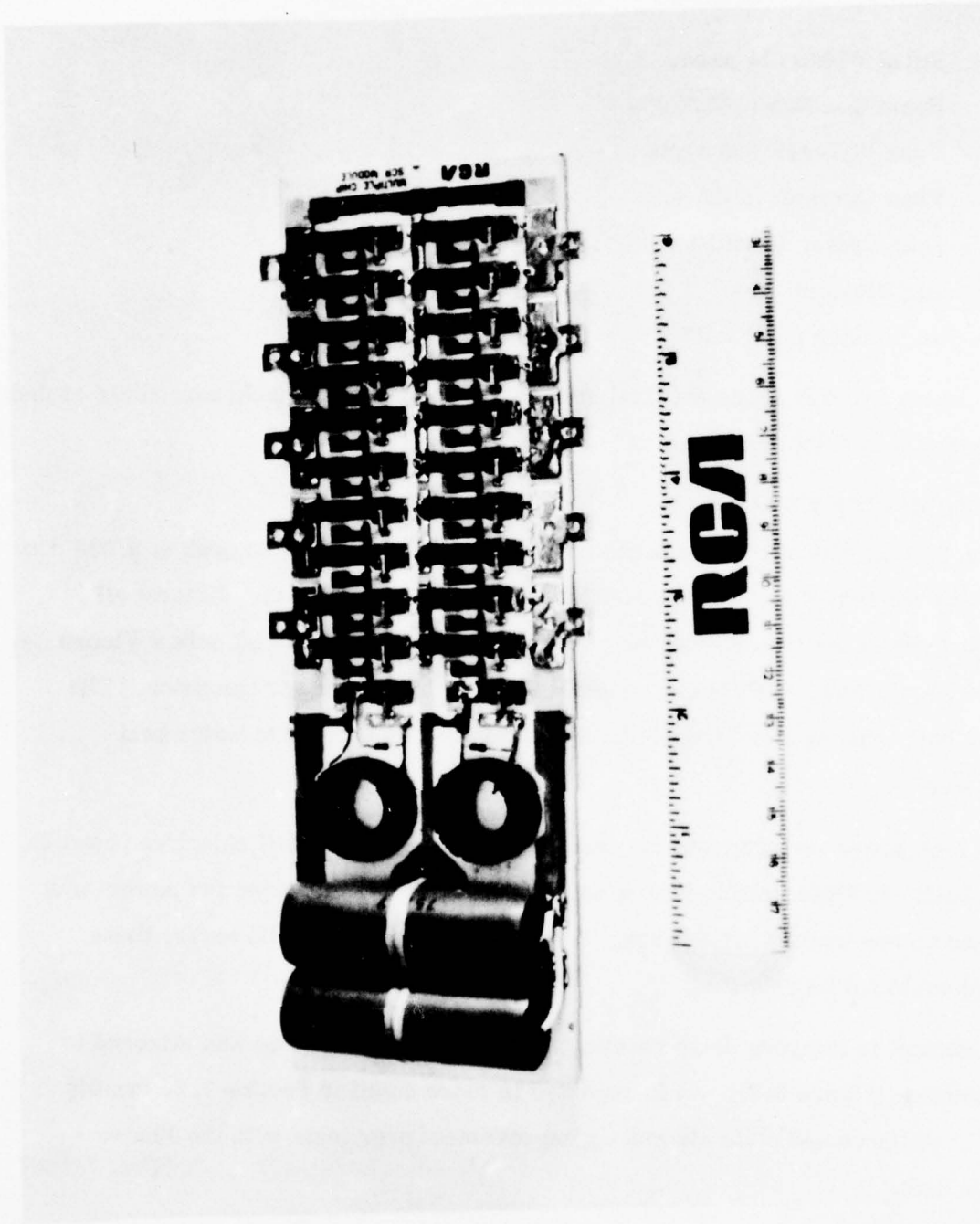


Figure 6-5. Assembled Multichip SCR Module

After the module passes the preliminary test, cooling fins are epoxied to the "back" of the substrate (one fin opposite each main SCR) as shown in Figure 6-6. Each half of the finned module is then put through a "final" screening test (to weed out any handling failures) with conditions as follows:

- Pulse Width: 14 μ sec.
- Repetition Rate: 66.7 pps
- Peak Voltage: 600 Volts
- Peak Current: 6 KA
- Duty Cycle: 0.00093
- Air Blast on Fins
- 15 minutes per "half"

The modules are now ready for final application: In a series stack; forced air cooled; or immersed in a cooling liquid (oil or freon).

6.3 LIQUID COOLED MODULE

For the highest peak and average power operation (6,000 amperes peak at 0.005 duty cycle) the modules may be immersed in a dielectric cooling bath. Mineral oil (univolt N-36 or equivalent) may be suitable for some applications, with a Fluoro Carbon Liquid (e.g., FC77) more suitable for the highest power operation. The cooling bath must in turn be cooled: For example, by a liquid to water heat exchanger.

Initial high power module tests revealed an inability to attain full objective power in an oil bath. In a circulating Fluoro Carbon bath (FC77), full objective power was obtained on one module for 4 hours. (Details in Section 7.2.) However, these results could not be repeated.

In an attempt to improve these results, a water cooled cold plate was attached to two modules (Figure 6-7). As is reported in more detail in Section 7.2, results with the water cooled plate showed no improvement over tests with the Fluoro Carbon bath.

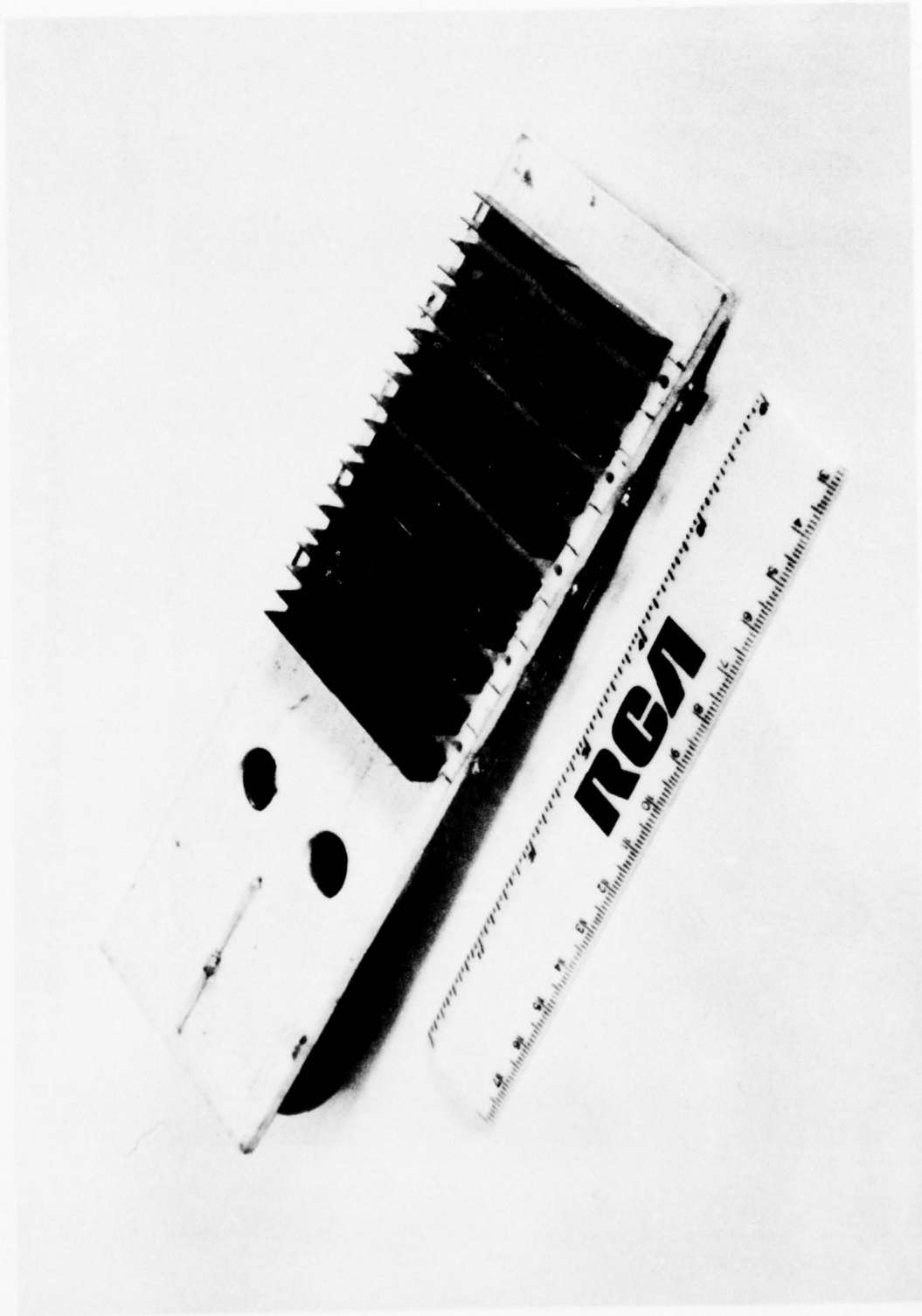


Figure 6-6. Module with Fins

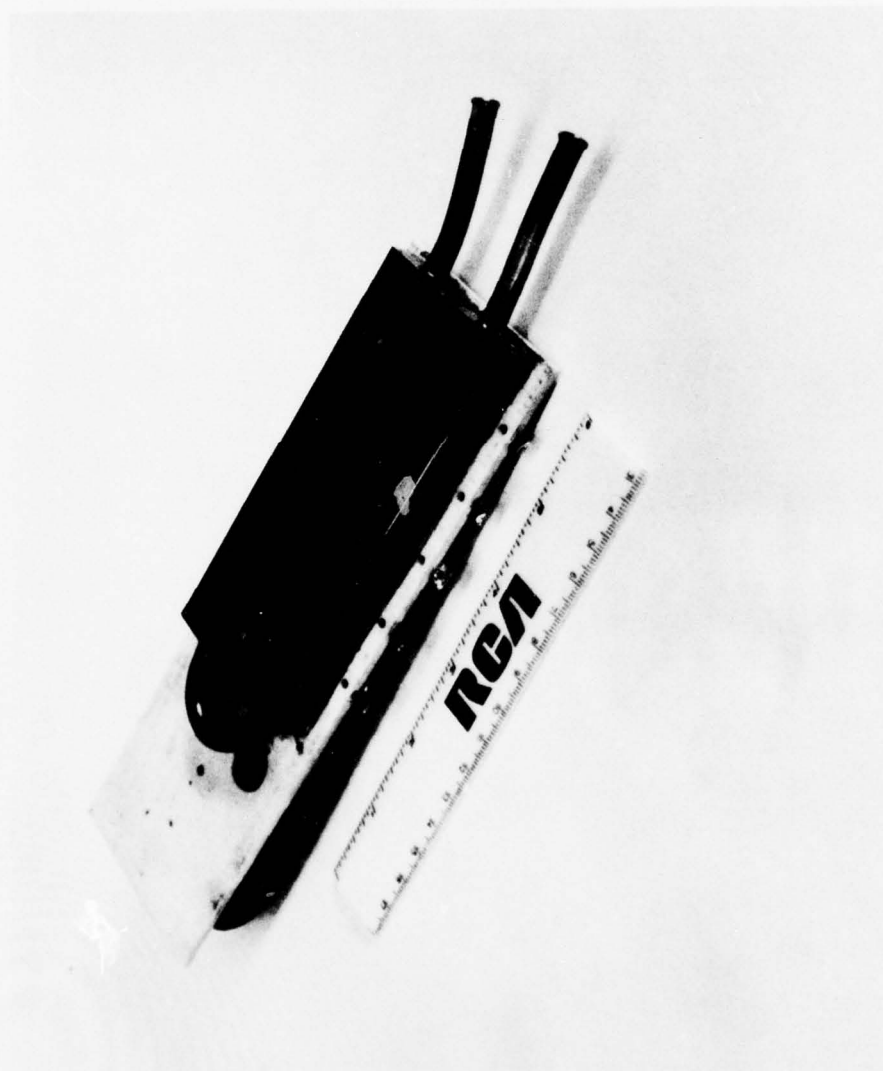


Figure 6-7. Module with Water-Cooled Cold Plate

6.4 SERIES STACK

Ten modules were assembled in a series stack to achieve a 10 kV (maximum) switch. Half of the modules in the series stack are fabricated in a "left hand" pattern in order to simplify the connections and minimize switch inductance.

Figure 6-8 is a photo of the assembled series stack. The High Voltage Trigger Isolation Cable is seen on the right, as it loops through the 20 trigger transformer toroids. The anode terminal (five eyelets) is on the left of the photo, and the cathode terminal (five similar eyelets) is at the right. A rotron "Tarzan" fan is attached to the rear of the assembly to draw cooling air past the modules.

When the switch is triggered, the current proceeds down the switch in a composite path shaped like a folded flat conductor: 4 inches wide by approximately 36 inches long before folding, 10 inches net length after folding. Symmetrical connections to the external circuit is important, to minimize current unbalance among the paralleled devices.

Figures 6-9 and 6-10 show the assembled series stack mounted in the 10 kV test set.

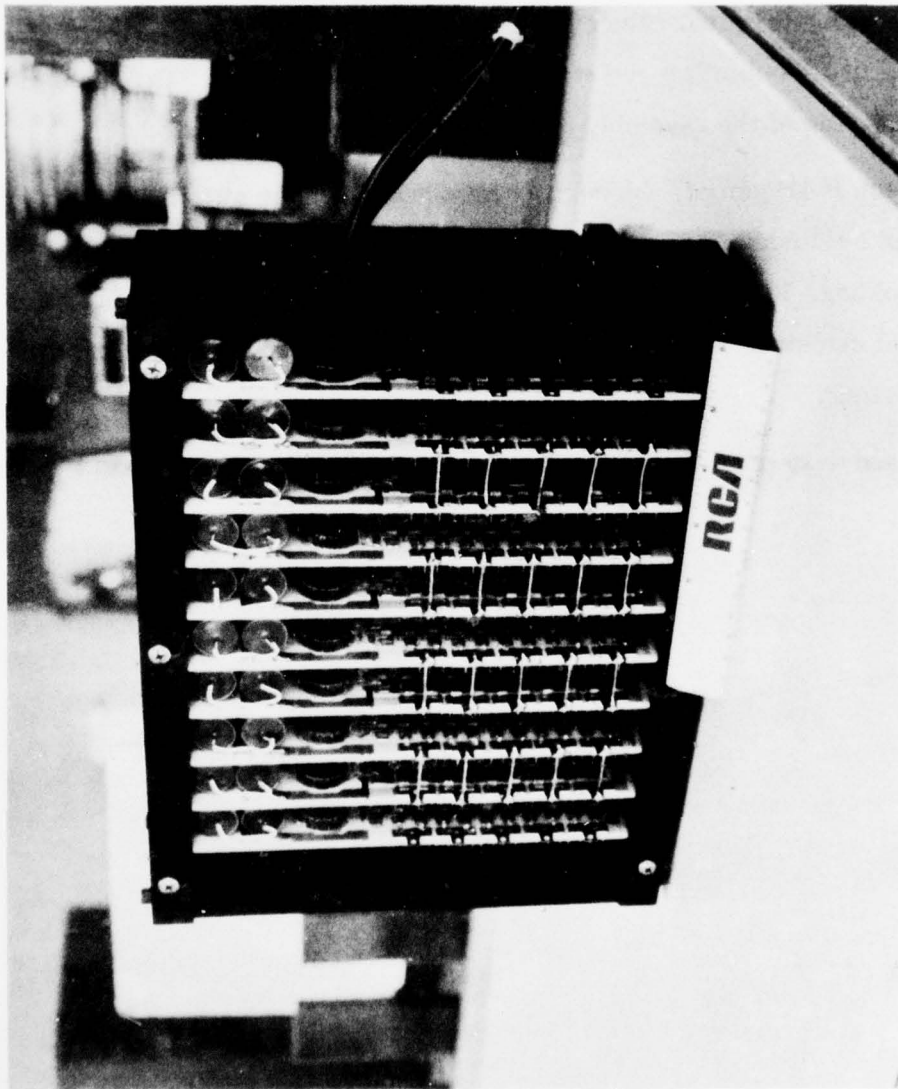


Figure 6-8. Ten kV Series Switch

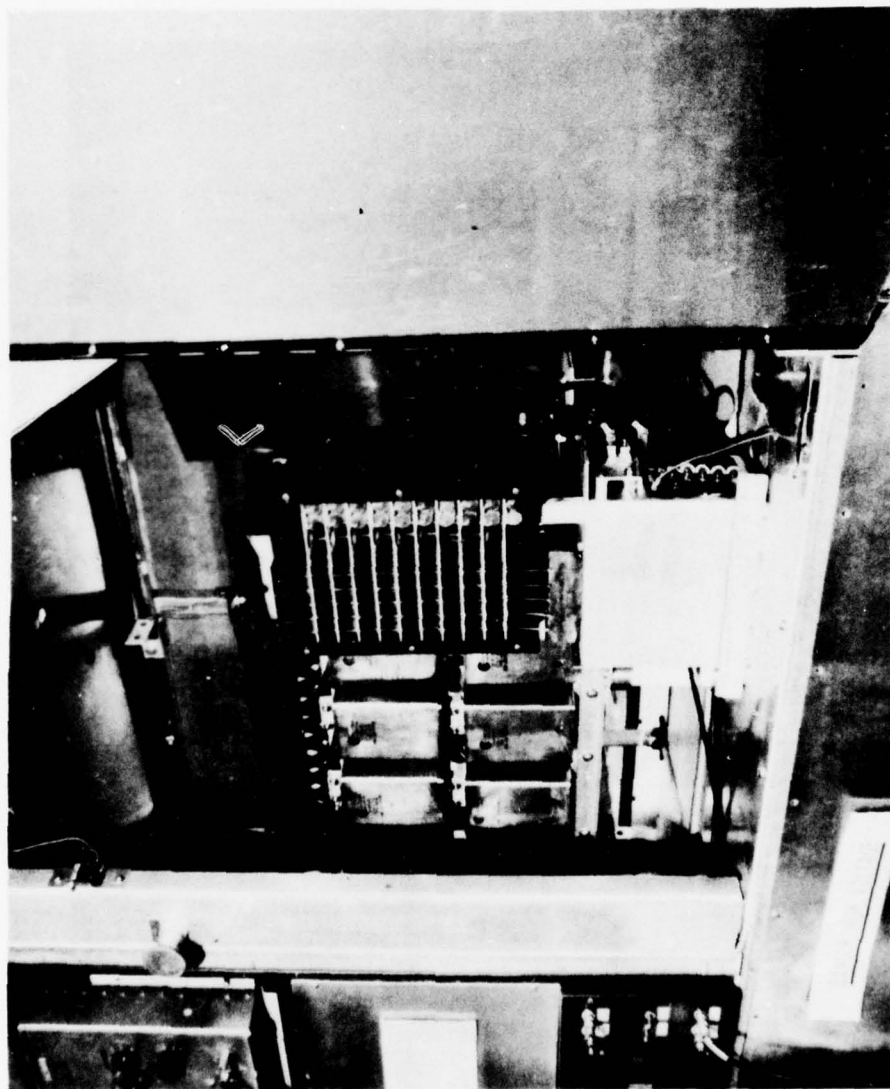


Figure 6-9. Ten kV Switch in Test Set

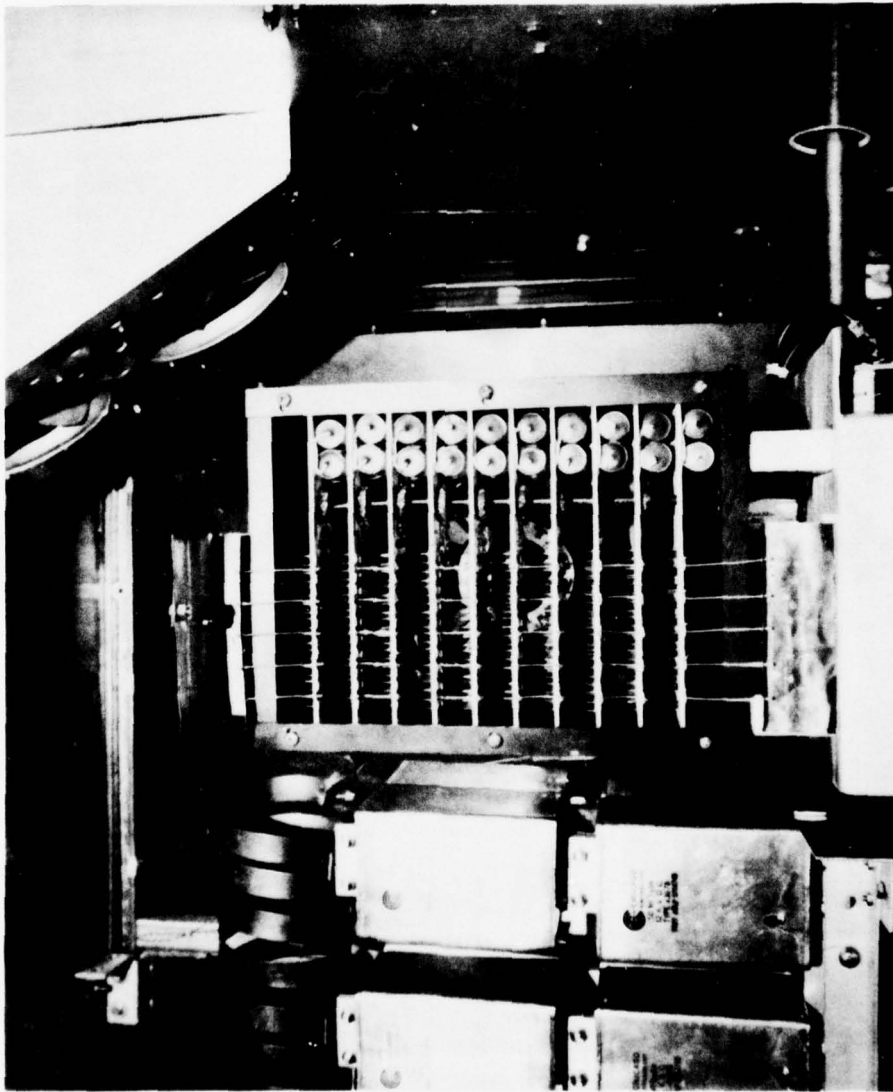


Figure 6-10. Ten kV Switch in Test Set

7.0 ELECTRICAL TESTS

7.1 LIQUID COOLED MODULE TESTS

The objective performance for a liquid cooled module is as follows:

Peak Voltage	1 KV
Peak Current	6 KA
Pulse Width	20 μ sec
Repetition Rate	250 PPS
Current Rise Time	1 μ sec
Duty Cycle	0.005
Peak Power	3 MW
Average Power	15 KW

The available test set limits the maximum value of several of these parameters as follows:

Peak Voltage	600 Volts
Current Rise Time	2-1/4 μ sec
Peak Power	1.8 MW
Average Power	9.0 KW

Module serial No. 2, without fins, was the first to undergo liquid cooling test. Initially the module was simply immersed in an oil bath which was, in turn, water cooled via copper tubing. Test parameters were as follows:

Pulse Width	20 μ sec
Repetition Rate	250 PPS
Rise Time	2-1/4 sec

In this test set, peak current is proportional to peak charging voltage: $I = 10 V$. The peak current was raised in 1,000 ampere steps. After 13 minutes at 4,000 amperes (400 volts peak), a failure occurred (4 chips failed short). Visual evidence of excessive temperature (bubbles driven out of substrate) preceded the failure by a few minutes.

The module was repaired, fitted with cooling fins, and used for the air cooled tests of Section 7.2.

The finned module (#2) was then re-installed in the oil cooling bath. This time, the switch was operated at full peak (600 volts peak and 6000 amperes peak), and the duty cycle raised in steps. After 13 minutes at 0.002 duty (20 μ sec pulse @ 100 PPS), a massive failure occurred which made further repair impractical.

This last result was somewhat surprising and discouraging. It was concluded that the fins did not assist with module cooling in an oil bath. The same module, with fins, failed in minutes in an oil bath the same test which it survived for 60 minutes in air.

Attention was now directed to obtaining a forced liquid flow across the module in the oil bath. Module serial No. 3 became available for the first forced liquid flow test on 16 November 1976. This was a bare module (no fins) in a forced oil cooling bath. The unit was operated at full peak (600 volts peak and 6 KA peak) and the duty cycle raised in steps by increasing the PRF. The unit operated 70 minutes at 0.004 duty (20 μ sec @ 200 PPS). At the end of this run, the substrate temperature measured 82.5°C in the center and 66°C at one end. The oil measured 61.5°C, and the cooling water measured 37°C.

The duty cycle was then raised to 0.005 (250 PPS) resulting in module failure in approximately 30 seconds: Three SCR chips shorted.

Module serial No. 3 was repaired and retested. This time, to obtain extra cooling effect, a forced circulation Fluoro Carbon bath (FC-77, boiling point 97°C) was used. After 57 minutes at full peak (6 KA and 0.004 duty cycle, three SCR chips failed short (not the same 3 as the previous failure).

Module serial No. 3 was repaired again, and the test repeated. On 24 November 1976, this module operated at the full 6 KA peak at 0.005 duty cycle for a cumulative total time of 4 hours (in two runs). Maximum substrate temperature was 73°C; maximum FC-77 temperature was 51°C.

Module serial No. 4 was completed and tested in the FC-77 bath. Following some initial difficulty (which was overcome), this module operated at full rating (6 KA peak at 0.005 duty) for slightly over 3 hours when a failure occurred. The module was repaired and retested three times; however, failure occurred quickly, at or near full rating, on each occasion.

These test results indicate that the module is on the verge of failure at 6 KA peak and 0.005 duty cycle. This could be a result of inadequate cooling, or could be a basic chip limitation.

In an attempt to obtain more effective cooling, Module serial No. 3 was fitted with a water cooled cold plate, attached to the "back" of the substrate by a thin coating of silicone adhesive. A full power test was run on 15 December 1976. Initial results were very encouraging as the substrate temperature was measured at 44°C (with 15°C water) compared to 73°C with the FC-77 coolant. After about 20 minutes at full power, two fuses blew in the hybrid circuit. Normal operation continued for an additional 3 minutes, when the operation was intentionally interrupted. The substrate temperature had increased to 47°C during these final 3 minutes. Examination showed that one SCR chip had shorted, and one fuse had opened in each parallel group, isolating the failed chip and one apparently good chip. Module serial No. 3 was then operated (with 9 surviving chips in parallel in each half) at 4.5 KA peak, 0.005 duty for over 4 hours (to demonstrate operation at 500 amperes average per chip, or equivalent of 5,000 amperes peak for a complete module).

In the hybrid SCR chip circuit, it is not possible to measure individual chip currents. However, it is possible to measure pulse currents in each of the five module terminal connections, with a "clip on" current transformer probe around the external bus wires. Repeated measurements on several modules show that the two outer bus wires consistently carry about 20% more than their share of the total current. It was theorized that this effect is a form of "Skin Effect" as applied to a broad flat conductor. In an attempt to neutralize this effect, a module (serial No. 14) was assembled with higher voltage SCR's in the outer positions and lower voltage SCR's in the center positions. This module (#14) was fitted with a water cooled cold plate and tested in mid April 1977. Pulse parameters were:

Pulse Width	20 μ sec
Current Rise Time	2-1/4 μ sec
Repetition Rate	250 PPS
Duty Cycle	0.005
Charging Delay	1.0 millisec
Charging Time	1.3 millisec
Peak Voltage	520 volts
Peak Current	5 KA
Peak Power	1.25 MW
Average Power	6.25 KW

Figure 7-1 shows photos of the pulse current and charging voltage waveforms.

This module (#14) was operated for a total of 8-1/2 hours at the 5 KA peak current level.

A second water cooled module (Serial No. 26) was tested at the same level, but failed (one shorted chip) after 22 minutes at 5 KA peak.

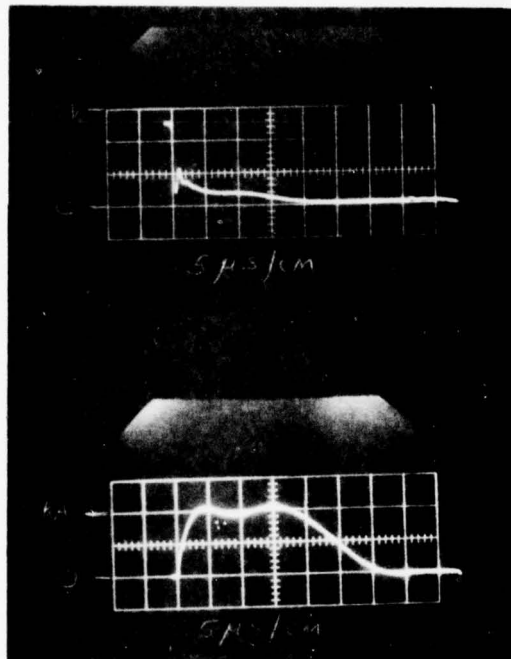
Module S/N 26 was repaired and retested on 20 May, operating at 5 KA peak and 0.005 Duty Cycle for 30 minutes. The B_2O_3 substrate temperature was 122°C at the center, and 61°C at one end, with 33.5°C cooling water temperature. S/N 26 was left in the test set for Performance Tests on 24 May.

At the conclusion of the testing period it seemed that the maximum current rating for 10 chips in parallel, at 0.005 duty, should be 5 KA rather than 6 KA.

7.2 AIR COOLED MODULE TESTS

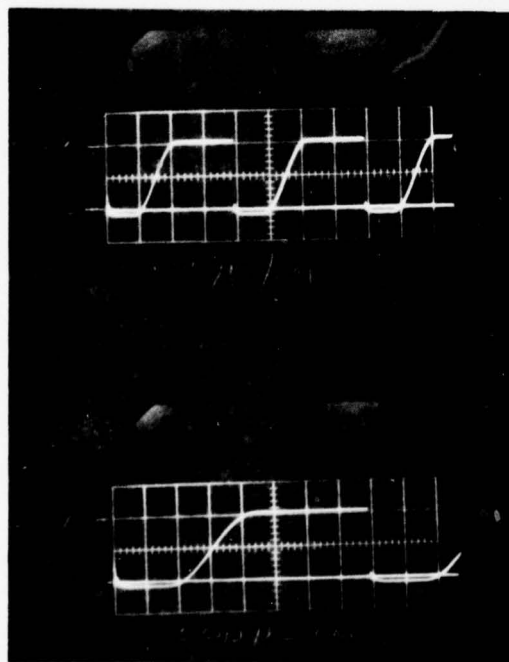
The objective performance for a forced air cooled module is as follows:

Peak Voltage	1 KV
Peak Current	3 KA
Pulse Width	10 μ sec
Repetition Rate	100 PPS
Current Rise Time	1 μ sec



- (a) Pulse Voltage Drop.
(1/2 Module)
Vertical: 100 V/cm
Horizontal: 5 $\mu s/cm$

- (b) Pulse Current
Vertical: 2.5 KA/cm
Horizontal: 5 $\mu s/cm$



- (c) Charging Voltage
Vertical: 250 V/cm
Horizontal: 1 ms/cm

- (d) Charging Voltage
Vertical: 250 V/cm
Horizontal: 500 $\mu s/cm$

Figure 7-1. Liquid Cooled Module Operating Waveforms

Duty Cycle	0.001
Peak Power	1.5 MW
Average Power	1.5 KW

Initial forced air cooled tests were made with module serial No. 2 with copper fins epoxied to the "back" surface (see Figure 6-6). Two successful runs were completed as follows:

<u>Parameter</u>	<u>Run #1</u>	<u>Run #2</u>	<u>Units</u>
Peak Voltage	600	600	Volts
Peak Current	6	6	KA
Pulse Width	20	20	μ sec
Repetition Rate	50	100	PPS
Current Rise Time	2-1/4	2-1/4	μ sec
Duty Cycle	0.001	0.002	
Peak Power	1.8	1.8	MW
Average Power	1.8	3.6	KW
Length of Run	2-1/2	1	Hours

Some of the parameters (peak voltage, pulse width, current rise time) were limited by the test set, and do not match objective figures. However, the results are encouraging because both peak current and duty cycle are twice the objective values for forced air cooled operation. The combination implies a switch dissipation 8 times the objective value (dissipation is proportional to I^2) (Du). The peak voltage (0.6 of objective value) and slow current pulse rise decrease switch stress, and thus act to moderate the enthusiasm generated by the overall result. Nevertheless, it is felt that these results show that the switch is easily capable of 3000 amperes peak at 0.001 duty.

7.3 TEN KV SERIES SWITCH TESTS

The ten KV series switch assembly was completed in late February 1977, and testing began on 28 February. The ten modules were arranged by serial number as follows: Anode End: 5, 20, 6, 21, 7, 22, 8, 23, 11, 24: Cathode End. Serial numbers above 20 are "left handed" (Reverse Pattern) modules.

The temperature of the lowest voltage substrate (serial No. 24) was monitored with a thermocouple near the middle.

Objective pulse parameters were:

- Pulse Width: 10 μ sec
- Current Rise Time: 1 μ sec
- Repetition Rate: 100 PPS
- Duty Cycle: 0.001
- Peak Voltage: 10 KV
- Peak Current: 3 KA
- Peak Power: 15 MW
- Average Power: 15 KW

Actual test set parameters were measured as follows:

- Pulse Width: 10 μ sec
- Current Rise Time: <1 μ sec
- Repetition Rate: 100 PPS
- Duty Cycle: 0.001
- Peak Voltage: 10 KV
- Peak Current: 2.8 KA
- Charging Delay: 1000 μ sec
- Charging Time: 400 μ sec
- Peak Power: 11 MW
- Average Power: 11 KW

After 37 minutes operation at this level, the series switch failed. Examination revealed at least one shorted chip in each parallel circuit, and a total of 38 failures in the 200 main SCR chips.

The modules were repaired, and a more rigorous screening procedure (module test) instituted to attempt to weed out potential failures before another series test (see Section 6.2 for description of screening tests). Some modules had to be repaired more than once, and one module was discarded as it was judged to be non-repairable.

The series switch was reassembled, adding a neon lamp indicator (in series with a 470 K ohm resistor) across each of the 20 series circuits (2 neon lamps per module). This allowed visual detection of shorted circuits while operating at high voltage, thus giving an opportunity to shut down for repair before extensive secondary failures could occur.

Other measures taken were as follows:

- Additional inductance was added to the input section of the pulse forming network, to increase the current pulse rise time to 1 μ sec.
- The load impedance was reduced 20% (to 1.17 ohms nominal) to insure a load current of at least 3 KA at full voltage, and to increase the PFN inverse voltage to aid switch recovery.
- The charging period was increased to about 650 μ sec.
- The charging delay was increased to 8-1/2 milliseconds, in order to reduce the time at full voltage.

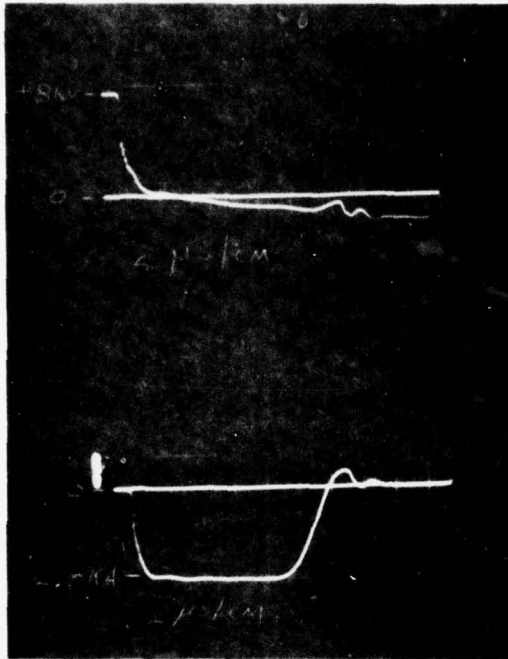
The next series switch operation was conducted on 25 March 1977. The neon indicators revealed shorts in two of the modules. These were repaired/replaced, and the series operation resumed on 7 April. The module order, by serial number was: Anode End: 6, 20, 7, 21, 8, 22, 9, 23, 10, 25: Cathode End.

In addition to monitoring the neon lamps, frequent oscilloscope measurements of voltage distribution were made during the series tests. The maximum operating level achieved was:

- Pulse Width: 10 μ sec
- Current Rise Time: 1 μ sec
- Repetition Rate: 100 PPS
- Duty Cycle: 0.001
- Peak Voltage: 8 KV
- Peak Current: 2.8 KA
- Charging Period: 600 μ sec
- Charging Delay: 8-1/2 millisecc
- Inverse Voltage: \approx 800 Volts
- Peak Power: 9.4 MW
- Average Power: 9.4 KW

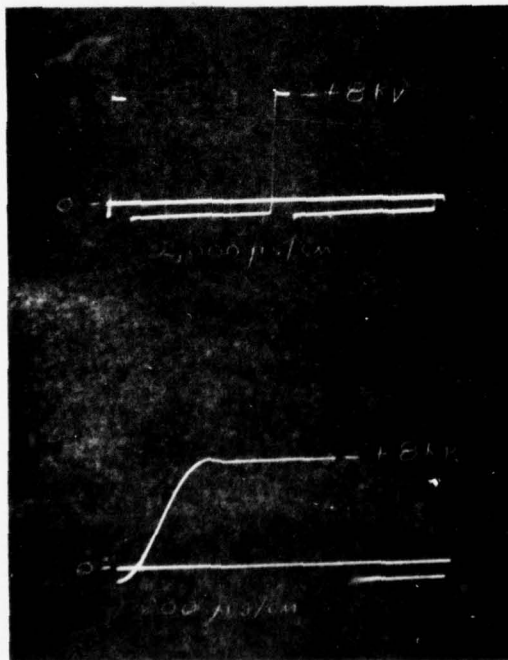
The test level was limited to 8 KV maximum in order to avoid danger of failure. This precaution was taken because of the short time period remaining to the Performance Tests.

Figure 7-2 shows oscilloscope photos of the pulse current and charging voltage waveforms. The maximum level noted above (8 KV/2.8 KA) was maintained for 2-1/2 hours on 12 April, and for an additional 2 hours on 18 April with no difficulty.



- (a) Pulse Voltage Drop
Vertical: 2.5 kV/cm
Horizontal: 2 μ s/cm

- (b) Pulse Current
Vertical: 1 kA/cm
Horizontal: 2 μ s/cm



- (c) Charging Voltage
Vertical: 2.5 kV/cm
Horizontal: 2 ms/cm

- (d) Charging Voltage
Vertical: 2.5 kV/cm
Horizontal: 200 μ s/cm

Figure 7-2. Series Stack Waveforms

8.0 PERFORMANCE TEST RESULTS

Performance Tests were conducted on 24 May 1977. Mr. J. Van Damme was present, representing Rome Air Development Center. The tests were divided into two portions: (1) Liquid Cooled Module and (2) Series Stack.

(1) Liquid Cooled Module:

Module S/N 26 was tested first, operating for 75 minutes at the following parameters:

Pulse Width:	20 microseconds
Current Rise Time:	2-1/4 microseconds
Repetition Rate:	250 pulses/second
Peak Voltage:	500 V
Peak Current:	5 KA

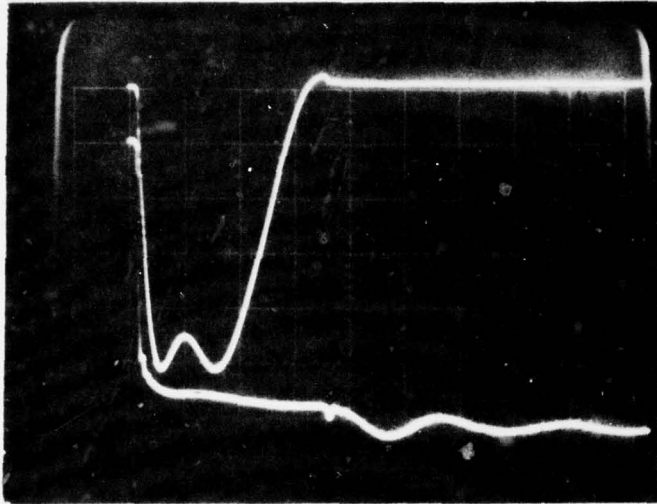
Pictures were taken of the pulse current and charging voltage waveforms. Figure 8-1(a) shows the pulse current waveform (top trace) and switch voltage waveform (bottom trace). Figure 8-1(b) shows the charging voltage waveform. The BeO substrate temperature was 112°C in the center and 60°C at one end with $25\text{-}1/2^{\circ}\text{C}$ water temperature.

S/N 26 was then removed and Module S/N 14 installed. Module S/N 14 was operated for approximately 5 minutes at 5 KA peak, 0.005 duty cycle. The BeO substrate temperature was 60°C in the center and 62°C at one end with 27°C water temperature. An attempt was made to raise the operating level to 6 KA peak, resulting in immediate module failure (shorted).

(2) Series Stack Test:

The Series Stack (ten modules in series) was operated for 53 minutes under the following conditions:

Pulse Width:	10 microseconds
Current Rise Time:	1 microsecond
Repetition Rate:	100 pulses/sec.
Peak Voltage :	8 KV
Peak Current:	2.8 KA



Vertical:

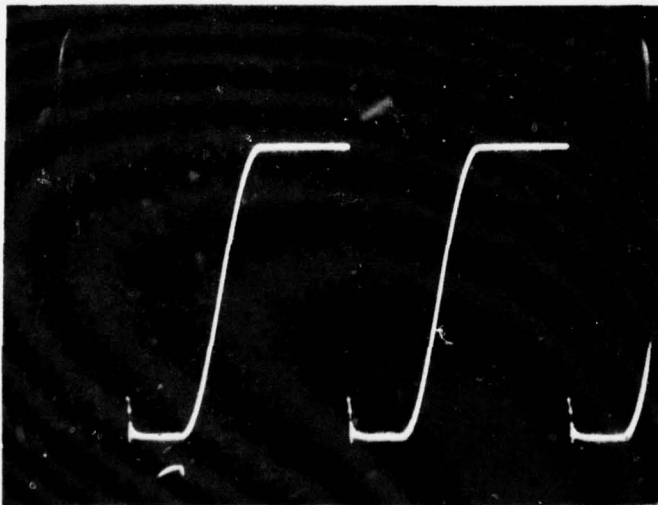
1 KA/cm

100 V/cm

Horizontal:

10 μ s/cm

(a) Pulse Current (Top Trace)
Voltage Drop (Bottom Trace)



Vertical:

100 V/cm

Horizontal:

1 ms/cm

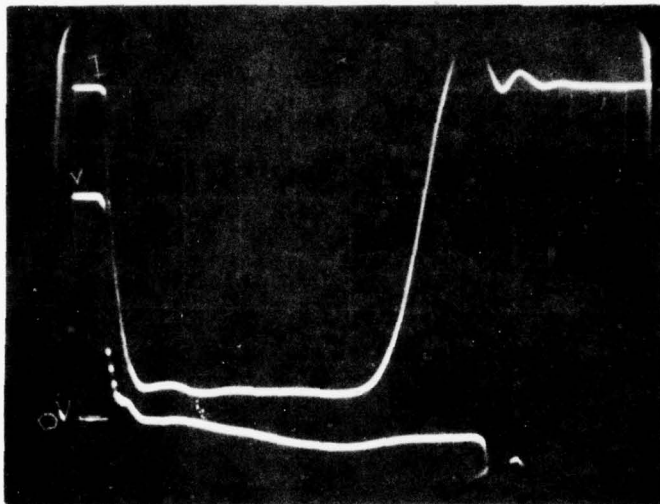
(b) Charging Voltage Waveform

Figure 8-1. Liquid Cooled Module Waveforms

Pictures were taken of this operation, which was interrupted by an HVPS problem (Variac failure). Figure 8-2 shows the operating waveforms. Figure 8-2 shows the pulse current waveform (top trace) and switch voltage (bottom trace). Figure 8-2(a), at 2 $\mu\text{sec}/\text{cm}$, shows the entire current pulse while Figure 8-2(b), at 0.5 $\mu\text{sec}/\text{cm}$, shows the rise time details. Figure 8-3 shows the charging voltage waveform at 200 $\mu\text{sec}/\text{cm}$ (Figure 8-3(a)) and at 2 millisecc/cm (Figure 8-3(b)). Following emergency repairs, the series air cooled switch was operated an additional 33 minutes with parameters as follows:

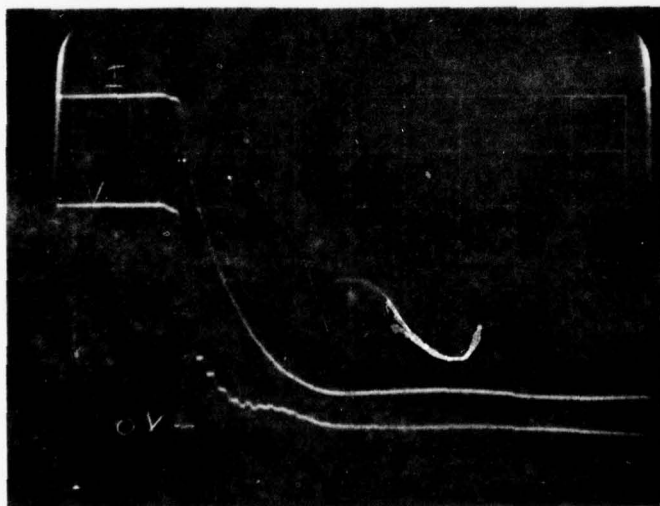
Pulse Width:	10 microseconds
Current Rise Time:	1 microsecond
Repetition Rate:	100 pulses/sec.
Peak Voltage:	8.9 KV
Peak Current:	3 KA
Load Resistance:	1.2 ohms
Peak Load Power:	10.8 MW
Average Load Power:	10.8 KW

Additional pictures were taken of this final operation, shown in Figures 8-4 and 8-5. Figure 8-4 shows the pulse current (top trace) and voltage drop (bottom trace) waveforms. Figure 8-5 shows the charging voltage waveform at 200 $\mu\text{sec}/\text{cm}$ (a), and at 2 millisecc/cm (b).



Vertical:
 500 A/cm
 2 KV/cm
 Horizontal:
 2 μ sec/cm

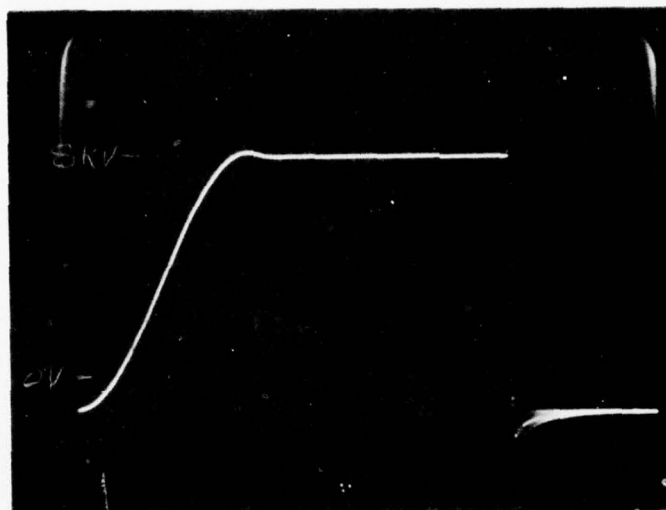
(a) Pulse Current (Top Trace)
 Voltage Drop (Bottom Trace)



Vertical:
 500 A/cm
 2 KV/cm
 Horizontal:
 0.5 μ sec/cm

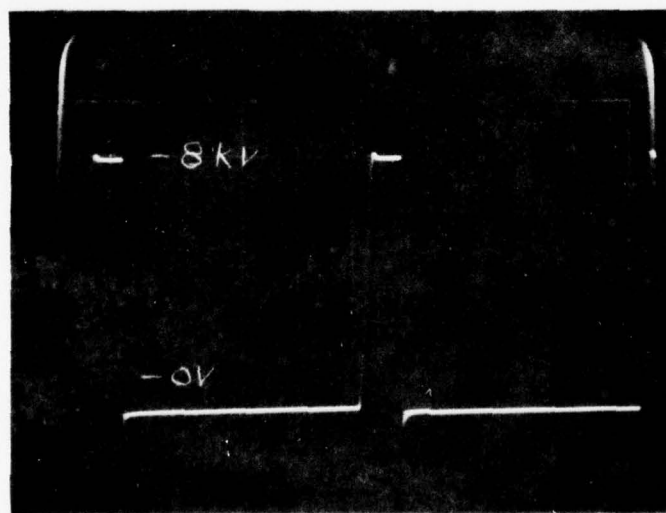
(b) Pulse Current (Top Trace)
 Voltage Drop (Bottom Trace)

Figure 8-2. Series Switch Pulse Waveforms



Vertical:
2 KV/cm

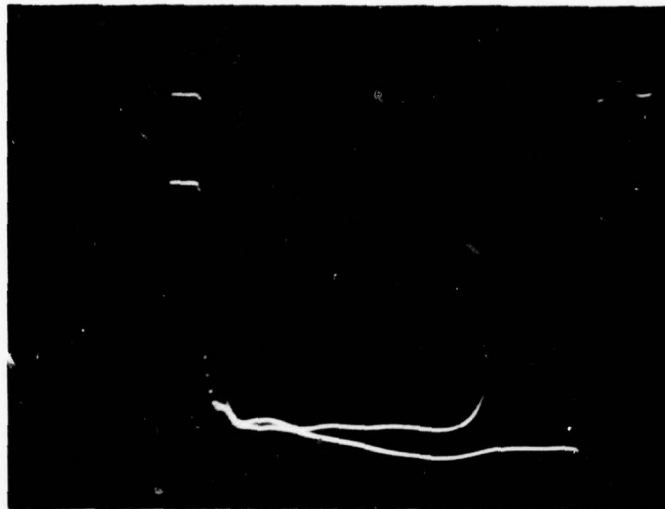
(a) Horizontal: 200 μ sec/cm



Vertical:
2 KV/cm

(b) Horizontal: 2 millsec/cm

Figure 8-3. Series Switch Charging Voltage Waveforms



Vertical:

500 A/cm

2 KV/cm

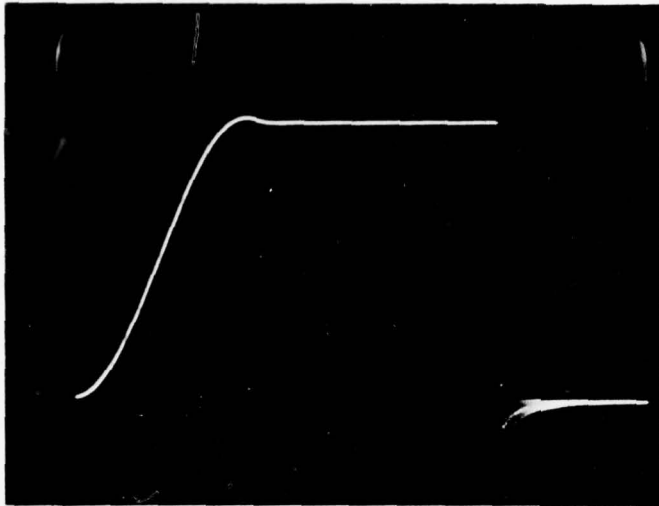
Horizontal:

2 μ sec/cm

Pulse Current (Top Trace)

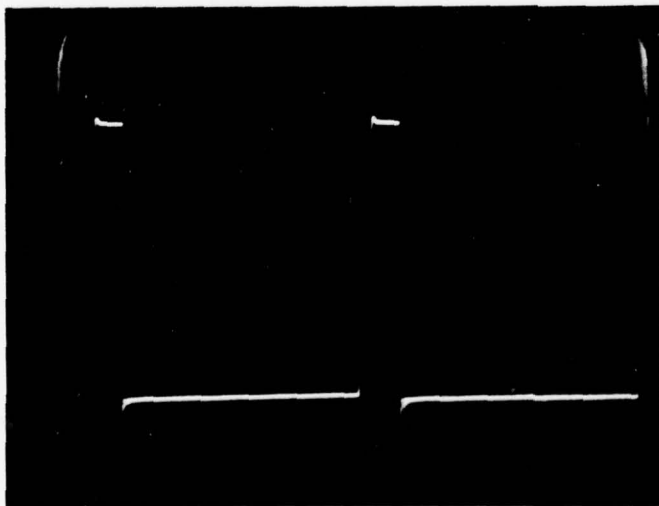
Voltage Drop (Bottom Trace)

Figure 8-4. Series Switch Pulse Waveforms



Vertical:
2 KV/cm

(a) Horizontal: 200 μ sec/cm



Vertical:
2 KV/cm

(b) Horizontal: 2 millsec/cm

Figure 8-5. Series Switch Charging Voltage Waveforms

9.0 CONCLUSIONS

Based on work done under preceding programs (References 2, 3, 5) RCA had previously concluded that high power solid state pulse modulators, using a multiplicity of small thyristors for the switch, are both feasible and desirable. This previous work was centered on packaged devices of the 2N3873 press fit type, which is a 600 volt maximum, 35 amperes RMS maximum device. A multiplicity of small devices has a di/dt advantage over a single large device, since the spreading distance is less.

The present program showed that utilization of small thyristor chips (40 amperes RMS rating) with hybrid circuit techniques can significantly reduce the size and weight of the thyristor switch. A size reduction of 3.5:1 in volume was achieved. Hybrid circuitry also has a potential manufacturing cost advantage over other techniques.

Difficulty was encountered in attaining sustained operation at the full objective ratings (6 KA peak current at 0.005 duty) for a liquid cooled module, and in attaining the full objective voltage rating in a series connected stack. A modest reduction in current and voltage ratings per chip results in a useful and practical hybrid switch.

Study of the test data shows that a large part of the difficulty in achieving full objective ratings was thermal in nature. Improvements in heat transfer (see Section 10) would improve current handling capacity at high duty cycles.

Summing up, the work performed under contract F30602-76-C-0197 demonstrated the usefulness of the Hybrid Multichip SCR Concept.

10.0 RECOMMENDED FUTURE PROGRAMS

It is recommended that effort be applied to improve the hybrid multichip SCR switch in the following areas:

(a) Improve heat dissipation:

- Solder on rather than epoxy on fins

As discussed in previous sections (5.4, 7.1, and 9.0), a severe thermal problem was encountered at the maximum objective rating of 6 KA peak current at 0.005 duty. It is felt that improvements in fin design, combined with solder rather than epoxy attachment (epoxy has poor thermal conductivity), could improve the thermal and electrical performance.

- Optimize substrate thickness

The thickness of the beryllia substrate is a compromise among several factors:

- It must be thick enough for mechanical strength.
- A thin substrate has less temperature drop through the thickness.
- However, a thicker substrate provides more spreading of heat, thus reducing thermal energy density.
- Cost is affected by thickness.

An analysis of the factors should be made to choose an optimum thickness.

- Determine optimum cooling liquid and cooling method.

(b) Fault indicator: Built in neon indicator lamps.

An indicator lamp in series with a resistor gives an instant visual indication of which modules in a series stack are operating normally, and which are shorted (no light). An LED (Light Emitting Diode) might be more suitable than a neon lamp.

(c) Match fuses to the RMS Current Requirement

The individual SCR fuses are currently sized for the maximum rating: 6 KA at 0.005 duty.

For lower peak currents and lower duty cycles, the fuse should be adjusted accordingly to assure prompt isolation of a failed SCR chip.

(d) Alternate chips

- Different vendor

The only vendor to respond with a suitable chip offer at the on-set of this contract was Unitrode. The field should be examined again to determine if other manufacturers can now offer suitable chips.

- Larger chips

A slightly larger chip (e.g., 0.250" square vs. 0.200" square) should be considered. Though time to full conduction would be slightly longer, total average dissipation might well be less.

It is also recommended that a demonstration application for a solid state modulator be funded. This could be a modest powered equipment . . . e.g., up to 5 Megawatts peak pulse power at 0.001 to 0.002 Duty cycle. An existing radar would be an ideal test vehicle. The object would be to demonstrate high reliability of the solid state modulator over an extended time period.

APPENDIX A

ROME AIR DEVELOPMENT CENTER
GRIFFISS AIR FORCE BASE
NEW YORK

STATEMENT OF WORK

FOR

MULTIPLE CHIP SCR

TABLE OF CONTENTS

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1.0	OBJECTIVE	A-1
2.0	SCOPE	A-1
3.0	BACKGROUND.....	A-1
4.0	TASKS/TECHNICAL REQUIREMENTS.....	A-2

1.0 OBJECTIVE

1.1 This is a program aimed at the development, fabrication and test of a new technique for compact packaging within one envelope, of a number of small silicon controlled rectifiers (SCRs). It is an objective to determine the most practical number of small inexpensive devices which can be mounted within a single package and be simultaneously triggered to enable their individual currents to be efficiently combined in the load circuit.

2.0 SCOPE

2.1 It is intended to develop techniques whereby a number of small SCR chips can be packaged in one package. The number of devices to be mounted within one envelope will be determined by the size of the package and reasonable limits of trigger complexity. It is also intended to investigate methods of triggering the multiple chips simultaneously so as to insure current and voltage equalization and still maintain as an objective, the fast rise time integrity inherent in the small device.

3.0 BACKGROUND

3.1 Lightweight tactical radar systems presently in Air Force inventory and proposed new systems have stringent size and weight specifications imposed upon them in order to meet mobility requirements. Most of these systems employ line type modulators because of their relative simplicity and low cost. Hydrogen thyratrons currently used in line type modulators of the megawatt class require a filament supply with several minutes warm up time, a high voltage system of diodes, inductors and pulse forming networks often insulated with oil to avoid high voltage corona. These components are heavy and are subject to failure due to vibration and mechanical shock. Recent development programs with high power switch modules utilizing many SCR devices in parallel indicate that SCR switches when properly configured for minimum size and weight will result in significantly improved switches for line type modulators. This program is an attempt to develop technology and circuitry to further improve devices to arrive at a low cost, low volume, highly reliable, high power switch.

4.0 TASKS/TECHNICAL REQUIREMENTS

4.1 The contractor shall provide engineering services, materials and facilities to perform the following:

4.1.1 Design, fabricate and test of a multiple chip silicon controlled rectifier.

4.1.2 The study shall include investigation of multiple chip configurations in typical standard packages such as flat packs or "hockey puck" types and/or hybrid assemblies on beryllia substrates or other materials of equal thermal characteristics.

4.1.3 The number of individual chips to be mounted within the package selected shall be determined by physical size and electrical isolation limitations.

4.1.4 In each package configuration the distribution of trigger signals shall be integral within the package. Entry of the trigger signal into the package shall incorporate means for direct current (dc) isolation when multiple packages are stacked in series for higher voltage operation.

4.1.5 The minimum chip size to be considered for this program shall be in the 600V, 600 Ampere range.

4.1.6 The objective ratings of the multiple chip package shall be:

- | | | |
|---------|--------------------|----------------------------|
| 4.1.6.1 | Hold off voltage | 600 volts |
| 4.1.6.2 | Peak pulse current | 6000 amperes |
| 4.1.6.3 | Minimum duty | .005 |
| 4.1.6.4 | Minimum pulsewidth | 20 μ sec |
| 4.1.6.5 | Service | Continuous |
| 4.1.6.6 | Current rise time | 10% to 90% in 1 μ sec. |

4.1.7 Design shall include control of the rise and fall time so as to be no worse than that of a single device.

4.1.8 The design of the thermal dissipation system shall include any effect on package size and provide means for stacking packages to enable series operation at high voltage without susceptibility to corona, arcing or serious current leakage through cooling system.

4.1.9 Delivery of ten (10) sample devices at end of contract to RADC.

4.1.10 Safety. A Preliminary Hazard List (PHL), Data Item DI-H-3278, shall be prepared by the contractor and delivered to the Government within 60 days after award of contract. This list shall address as a minimum the checklist items contained in the Checklist of General Design Criteria, AFSC DH 1-X DN6B5. Particular attention should be given to the potential hazard areas of high voltage and X-ray radiation. A Preliminary Hazard Analysis (PHA) may be directed by the Air Force for significant items identified in the PHL.

APPENDIX B
OPERATING INSTRUCTIONS

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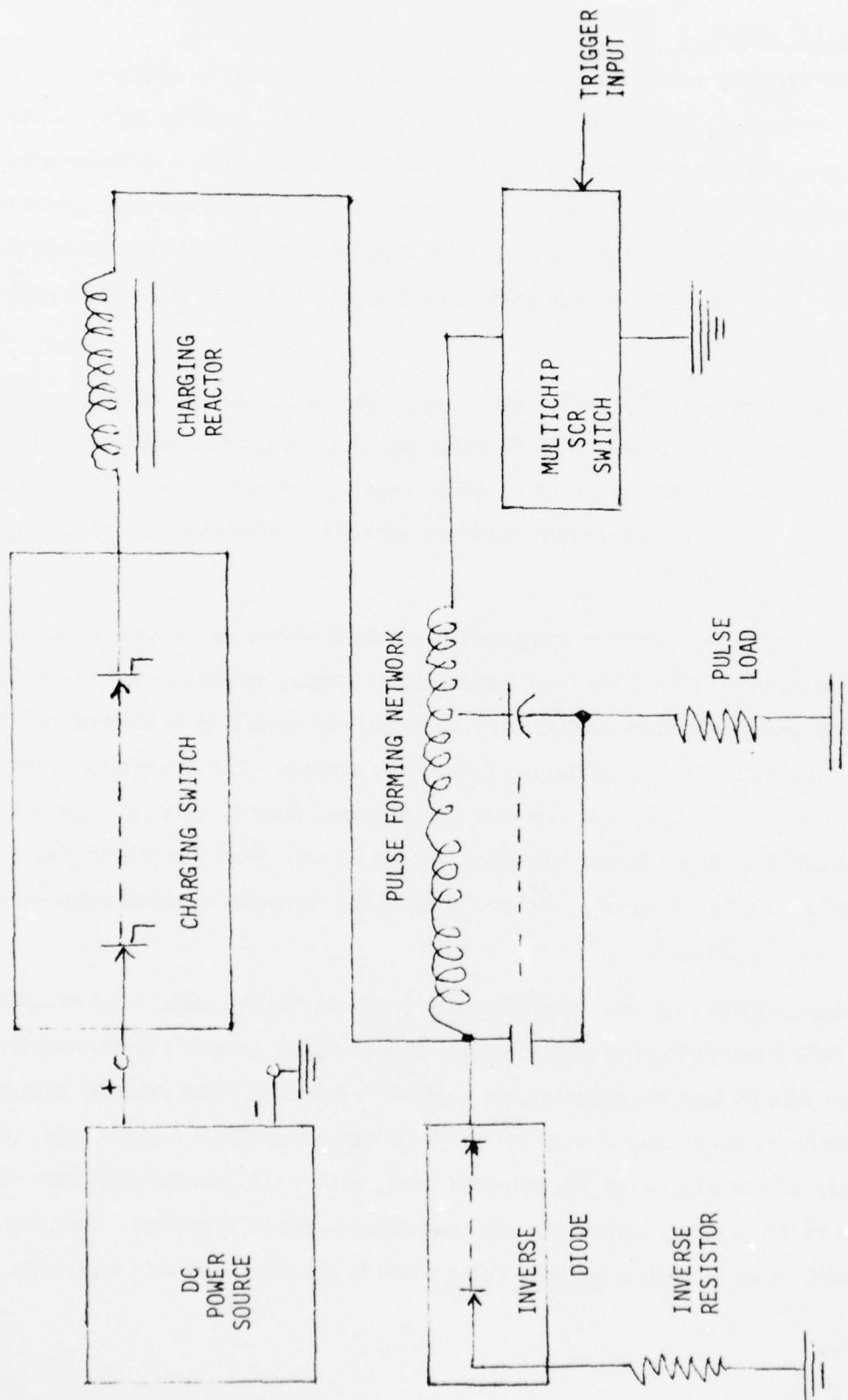
A. SINGLE MODULE

The multichip SCR switch modules are suitable for operation in artificial line type modulator circuits, such as is illustrated in Figure B-1. Suitable pulse widths may vary from a few microseconds to dozens of microseconds, with a pulse current rate of rise not-to-exceed $6 (10^9)$ amperes per second. Peak pulse current should not exceed 6,000 amperes. RMS current, with liquid cooling, should not exceed 350 amperes. Peak charging voltage (peak switch **voltage**) should not exceed 1,000 volts for a single module.

The circuit parameters should be chosen to provide a 10% to 15% inverse voltage on the PFN following the pulse. The charging switch shown, while not absolutely necessary in all cases, is suggested as an aid to switch recovery, especially if a matched end of line clipper is used. Fault circuitry should be included to electronically interrupt pulsing if the load arcs.

Physical arrangement is very important in order to obtain equal current division among the ten paralleled chips. Minimal length, equal length, and symmetrical connections should be made to each of the five main terminals on each side of the switch. Figure 6-5 shows the circuit side of the multichip SCR module. The anode side of each chip may be identified as the short bus with fuse attached (next to ruler in Figure 6-5). The cathode side has a longer bus strip without a fuse. Note that Figure 6-5 shows the regular, or "right hand", pattern. Half of the delivered modules have a reversed, or "left hand", pattern.

Two trigger toroids are shown in Figure 6-5; one to trigger each of the two pilot SCR's (i.e., SCR 1 and SCR 12 of Figure 4-2). These trigger toroids are current transformers with 50 turn secondaries and a one turn primary. The primary turn should be a minimum sized loop of wire with high voltage insulation. A short pulse (3 to 5 μ seconds) of current, 50 to 100 amperes peak, with $<1/2$ second rise time, is applied to the primary turn to initiate conduction in the SCR module. Polarities should be chosen so as to apply a positive going pulse to the pilot SCR gate electrode.



B-2

Figure B-1. Artificial Line Type Modulator

A convenient method of triggering a single module is to couple a third trigger toroid to the high voltage primary trigger wire, and to apply a 50 volt (minimum) 50 ohm (maximum) pulse to the terminals of this auxiliary toroid. Check polarities with a scope before applying anode voltage to the module.

B. TEN kV SERIES SWITCH

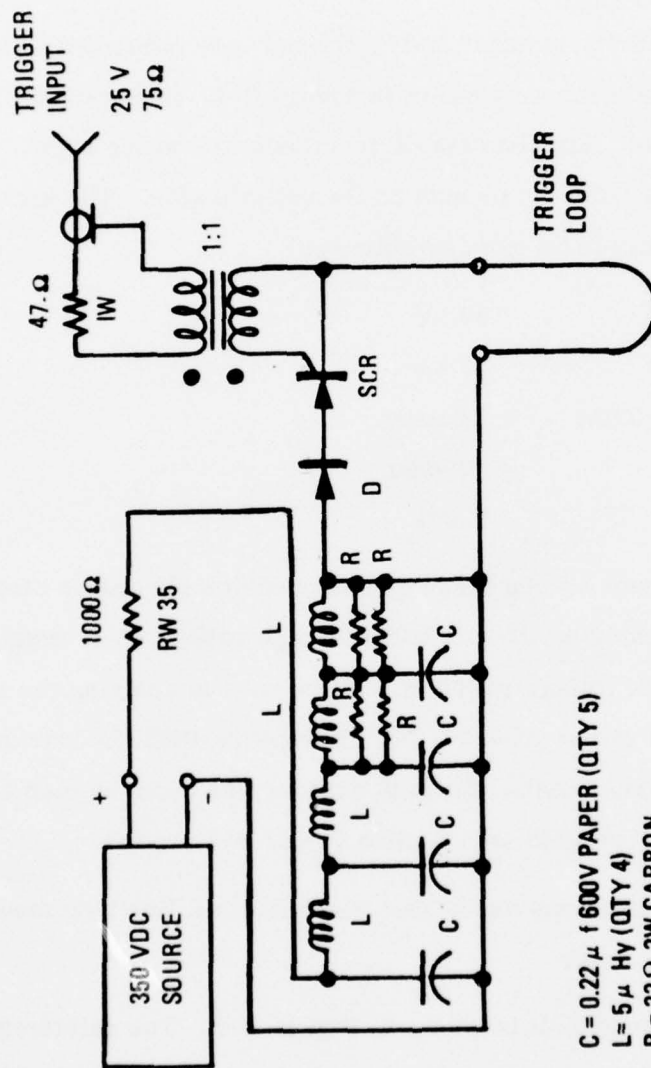
Ten modules, five each "right hand" and "left hand" are connected in series and installed in an air cooled plenum as shown in Figure 6-7. In Figure 6-7, the anode terminals are on the left, and the cathode terminals are on the right. The primary trigger wire protrudes from the plenum on the cathode side. The air cooled series switch of Figure 6-7 was to be rated as follows:

- Peak Voltage 10 kV
- Peak Current 3 kA
- Current Rise Time 1 μ sec
- Pulse Width 10 μ sec
- Duty Cycle 0.001

Voltage division problems among the 10 series modules (20 series circuits) has caused some difficulty with achieving the full 10 kV voltage rating. It is suggested that an absolute maximum peak voltage rating of 8 kV be used in applying the series switch. The 3 kA peak current rating (at 0.001 Du; 95 amperes RMS) is considered to be conservative; in single module tests, the peak current was taken as high as 6 kA peak at 0.002 Du, or 268 amperes RMS (see Section 7.1 of this report).

Otherwise, normal precautions associated with artificial line type modulators, as discussed in (a) above, apply.

A recommended trigger circuit is shown in Figure B-2. The relatively high voltage (350 volts) is specified to minimize rise time problems associated with circuit inductance. The triggering circuit should be energized, and pilot SCR gate trigger polarity observed (on a convenient pilot SCR) with an oscilloscope before applying anode voltage to the switch. If the gate polarity is negative, reverse the connections to the primary trigger loop.



C = 0.22 μ f 600V PAPER (QTY 5)
 L = 5 μ Hy (QTY 4)
 R = 22 Ω 2W CARBON
 D = D2540M OR EQUIV.
 SCR = 2N3899

Figure B-2. Trigger Circuit

APPENDIX C

MULTIPLE CHIP SCR

DATA ITEM DI-H-3278

PRELIMINARY HAZARD LIST

DATA ITEM DI-H-3278
PRELIMINARY HAZARD LIST
FOR
MULTIPLE CHIP SCR

The hazards associated with electronic equipment operation may be divided into two broad categories:

- (1) Hazards to operating personnel.
- (2) Hazards to the equipment.

The multiple chip SCR switch is essentially a high voltage component for use in high voltage, high power pulsed equipment. As such, the hazards of high voltage and X-ray radiation require particular attention.

The high voltage hazard will be minimized by proper application of interlocks in the equipment enclosure which contains the multiple chip SCR. Capacitor bleeder resistors and/or shorting switches will be incorporated in the equipment to remove hazardous voltages when the equipment is opened.

A careful analysis shows that X-rays will not be emitted by the multiple chip SCR. This is so for two reasons:

- (1) The voltage across any one element is 600 volts maximum, below the level required for generation of X-rays.
- (2) In the semiconductor devices, electrons are not accelerated through a vacuum to high velocities, to then impinge on a metal target, as is the case in high power vacuum tubes which generate X-rays. Thus, the basic mechanism for X-ray generation is absent.

The following checklist of additional potential hazards is taken from design note 6B5 of AFSC DH 1-X, "Checklist of General Design Criteria".

The design of the multiple chip SCR will comply with all applicable items as shown by the attached check list.

DESIGN NOTE 6B5 ELECTRICAL ELECTRONIC EQUIPMENT AND SYSTEMS

INSTRUCTIONS

In each block mark:

"Y" — For YES, if included in this design;
"N" — For NO, if not included in this design;
"N/A" — When NOT APPLICABLE to this design.

The letters (A, S, and/or M) after an item indicate applicability; i.e., (A) — Aircraft, (S) — Spacecraft, (M) — Missiles.

Entries in the "REFERENCES" column refer to DH 1-6, System Safety, except where noted.

CONTENTS

1. SAFETY DESIGN CONSIDERATIONS
2. INSTALLATION AND MAINTENANCE
3. GENERAL CONSIDERATIONS FOR SYSTEMS
4. TESTING

1. SAFETY DESIGN CONSIDERATIONS		REFERENCES
<input type="checkbox"/>	1.1 Select materials for electrical/electronic equipment in accordance with equipment specification or as specified in MIL-E-4158.	4E1-2 MIL-STD-143
<input type="checkbox"/>	1.2 Ensure that flammable materials are not specified for use in the system.	4E1-2
<input type="checkbox"/>	1.3 Select materials that will not liberate gases or fumes which are toxic, corrosive, flammable, or explosive under any combination of specified service conditions.	4E1-2
<input type="checkbox"/>	1.4 Do not use dissimilar metals in intimate contact unless suitable corrosion protection is provided.	4E1-2

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1. SAFETY DESIGN CONSIDERATIONS (CONTD)		REFERENCES
<input type="checkbox"/>	1.5 Do not use glass fiber materials where they may cause skin irritation.	4E1-2
<input type="checkbox"/>	1.6 Use insulating and jacketing compounds in cordage and cabling that exhibit long life without degradation of performance under the anticipated service conditions.	4E1-3.1
<input type="checkbox"/>	1.7 Derate power cordage and cable when operating ambient temperatures exceed 30°C.	4E1-3.1
<input type="checkbox"/>	1.8 Hold wiring termination points to a minimum.	4E1-3.2
<input type="checkbox"/>	1.9 To prevent accidental body contact, cover or protect high-voltage terminals located near components which are frequently worked on.	4E1-3.2.1
<input type="checkbox"/>	1.10 Protect terminal points from shorting by foreign objects and debris, and from possible circuit degradation by dirt, moisture, or other contaminants.	4E1-3.2.1
<input type="checkbox"/>	1.11 Space terminals to which wires are soldered far enough apart so that work on one terminal does not damage another.	4E1-3.2.1
<input type="checkbox"/>	1.12 Ensure that the moisture-excluding property of potted parts is not degraded by normal soldering operations on terminals.	4E1-3.2.1
<input type="checkbox"/>	1.13 Provide adequate spacing or barriers to prevent corona breakdown or low-leakage resistance under specified service conditions.	4E1-3.2.1
<input type="checkbox"/>	1.14 Select terminals that will not turn or loosen when subjected to certain service conditions.	4E1-3.2.1
<input type="checkbox"/>	1.15 Ensure that wiring terminals are sufficiently strong to support the wires attached and to ensure necessary fabrication and maintenance operations.	4E1-3.2.1
<input type="checkbox"/>	1.16 Avoid connectors with unkeyed symmetrical pin arrangements.	4E1-3.2.2
<input type="checkbox"/>	1.17 Provide alignment pins, keyway arrangements, or similar features on adjacent connectors to prevent cross-connection.	4E1-3.2.2
<input type="checkbox"/>	1.18 Furnish articles of equipment likely to require future additional circuits with connectors having spare contacts in accordance with MIL-STD-454.	4E1-3.2.2
<input type="checkbox"/>	1.19 Terminate connectors so that receptacle pins are "hot" and plug pins are "cold."	4E1-3.2.2

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2

I. SAFETY DESIGN CONSIDERATIONS (CONTD)		I. SAFETY DESIGN CONSIDERATIONS (CONTD)		REFERENCES
<input checked="" type="checkbox"/>	1.20	Furnish caps or covers to keep unmated connectors from contamination.	<input checked="" type="checkbox"/>	4E1-3.2.2
<input checked="" type="checkbox"/>	1.21	Use connections for connector termination where practicable.	<input checked="" type="checkbox"/>	4E1-3.2.2
<input checked="" type="checkbox"/>	1.22	Ensure that layout and spacing of connectors permit ease of connection and disconnection when using appropriate tools.	<input checked="" type="checkbox"/>	4E1-3.2.2
<input checked="" type="checkbox"/>	1.23	Include assembly instructions in the design for connectors which require special tools or processes.	<input checked="" type="checkbox"/>	4E1-3.2.2
<input checked="" type="checkbox"/>	1.24	Color code chassis wiring in accordance with MIL-STD-481.	<input checked="" type="checkbox"/>	4E1-3.3
<input checked="" type="checkbox"/>	1.25	Identify equipment assemblies and parts in accordance with MIL-STD-130.	<input checked="" type="checkbox"/>	4E1-3.3
<input checked="" type="checkbox"/>	1.26	Ground inactive wires installed in long lines (conduit or cable) to allow for stray or static electricity discharge.	<input checked="" type="checkbox"/>	4E1-3.4
<input checked="" type="checkbox"/>	1.27	On plug and convenience outlets for portable tools and equipment, include provisions for automatically grounding the case of such equipment when the plug is mated to the receptacle.	<input checked="" type="checkbox"/>	4E1-3.4
<input checked="" type="checkbox"/>	1.28	Do not use shields, excepting coaxial cables, as a current-carrying ground connection.	<input checked="" type="checkbox"/>	4E1-3.4
<input checked="" type="checkbox"/>	1.29	Design and construct the equipment to ensure that all external parts, surfaces, and shields, exclusive of antenna and transmission line terminals, are at ground potential at all times during normal operation.	<input checked="" type="checkbox"/>	4E1-3.4
<input checked="" type="checkbox"/>	1.30	Ensure that the design considers ground faults and voltage limits established on a basis of hazardous location.	<input checked="" type="checkbox"/>	4E1-3.4
<input checked="" type="checkbox"/>	1.31	Specify that the ground connection to the chassis or frame provides a corrosion-resistant connection.	<input checked="" type="checkbox"/>	4E1-3.4.1
<input checked="" type="checkbox"/>	1.32	Terminate shielding a sufficient distance from exposed conductors to prevent shorting or arcing between the conductor and the shielding.	<input checked="" type="checkbox"/>	4E1-3.4.2
<input checked="" type="checkbox"/>	1.33	Secure shielding adequately to prevent contact with exposed current-carrying parts.	<input checked="" type="checkbox"/>	4E1-3.4.2
<input checked="" type="checkbox"/>	1.34	Provide primary circuits and cables with overload devices to protect against damage by fire, explosion, or overheating due to electrical overload.	<input checked="" type="checkbox"/>	4E1-3.5

1. SAFETY DESIGN CONSIDERATIONS (CONTO)

REFERENCES

1. SAFETY DESIGN CONSIDERATIONS (CONTO)

REFERENCES

- 1.50 ☐ N/A Design equipment exhibiting a radiation hazard (e.g., micro-wave or X ray) within the limits of MIL-R-9673.
- 1.51 ☐ N/A Provide discharging devices to discharge high voltage capacitors and capacitors unless they discharge to 30 V DC within 2 sec or less.
- 1.52 ☐ N/A Ensure that these protective devices are positive acting, highly reliable, and actuate automatically when the case or rack is opened.
- 1.53 ☐ N/A Ensure that shorting bars are actuated either by mechanical release or by an electrical solenoid when the door or cover is open.
- 1.54 ☐ N/A When resistive bleeder networks are used to discharge capacitors, ensure that the bleeder network consists of at least two equal valued resistors in parallel.
- 1.55 ☐ N/A The particular discharging device that is chosen must insure that the capacitor is discharged to 30 V DC within 2 sec.
- 1.56 ☐ N/A Ground or insulate controls, control shafts, knobs, or levers to prevent shock or burns to personnel.
- 1.57 ☐ N/A Ascertain that the temperature of front panels and operating controls does not exceed 43°C at an ambient temperature of 25°C.
- 1.58 ☐ N/A Ensure that the temperature of exposed parts and equipment enclosures which may be contacted by operating personnel does not exceed 60°C at an ambient temperature of 25°C.
- 1.59 ☐ N/A Locate, recess, or guard critical switches, breakers, and similar controls in a manner to prevent accidental displacement or activation.
- 1.60 ☐ Y Design mechanical linkage, instrument leads, and electrical connections to positively prevent inadvertent reversing or cross connection.
- 1.61 ☐ N/A Avoid sharp projections, corners, or edges on cabinets, doors, hinged covers, and similar parts of equipment.
- 1.62 ☐ N/A Guard or protect all rotating mechanical parts such as gears, fans, and bolts when the equipment is complete and operating.
- 1.63 ☐ N/A Protect personnel from possible injury from implosion of cathode-ray tubes.

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- 1.64 ☐ N/A In the event of meter failure, assure that meters possess overload bypass or alternate features to eliminate high-voltage potential at the meter terminals.
- 1.65 ☐ N/A Do not specify metal ladders for use around electrical/electronic equipment and facilities.
- 1.66 ☐ Y Provide adequate equipment cooling for performance under any combination of service conditions.
- 1.67 ☐ N/A Locate or configure ventilation holes so that foreign objects cannot be inserted inadvertently to contact high-voltage sources.
- 1.68 ☐ Y Design equipment to withstand any probable combination of environmental conditions without mechanical or electrical malfunction.
- 1.69 ☐ Y Use inherently safe (e.g., explosion proof, dustproof, moisture-proof) equipment in all hazardous environments.

2. INSTALLATION AND MAINTENANCE

- 2.1 ☐ N/A Provide proper equipment accesses to all points, units, and components which may require testing, adjustment, maintenance, or repair.
- 2.2 ☐ N/A Locate accesses away from dangerous mechanical or electrical components where possible; otherwise, placard such accesses as to the potential hazard.
- 2.3 ☐ N/A Furnish accesses with internal fillets, or with rubber, fiber or plastic if they might injure the operator's hands or arms.
- 2.4 ☐ N/A Provide screwdriver guides to adjustment point which must be operated near high voltages.
- 2.5 ☐ N/A Position equipment components and wiring to prevent damage from opening and closing the assembly.
- 2.6 ☐ Y Ensure that units are small and light enough for one man to carry and handle, whenever this is feasible.
- 2.7 ☐ N/A Provide convenient handles on units to assist in removal, replacement, or carrying.

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CHAP 6 - SYSTEM SAFETY
SECT 6B - AEROSPACE GROUND AND
ANCILLARY EQUIPMENT

AFSC D4 1-X
DN 6B5

AFSC D4 1-X
DN 6B5

CHAP 6 - SYSTEM SAFETY
SECT 6B - AEROSPACE GROUND AND
ANCILLARY EQUIPMENT

AFSC D4 1-X
DN 6B5

3 GENERAL CONSIDERATIONS FOR SYSTEMS (CONTD) REFERENCES

N/A	3.2	Design battery vent outlets to eliminate vent system back flow and to prevent battery acid from being ejected from the vent outlet.	3H1-6.6
	4.1	Ensure that system verification test circuits do not indicate the command, rather, that they indicate the system's actual response.	3H3-2.1
	4.2	Design system monitors and test circuits so that no hazard to the crew is presented.	3H3-2.1
	4.3	Provide that power application will not actuate critical circuits as a result of function switches which may be cycled without indicating the on-off position during a power-off phase (i.e., push on/push off switches).	3H3-2.1
N/A	4.4	Provide continuous monitoring for tests requiring judgments rather than standards.	3H3-2.2

4. TESTING

2. INSTALLATION AND MAINTENANCE (CONTD)

N/A	2.8	Provide rests, stands, or other protectors to prevent damage to delicate parts when elements of the equipment are removed for repair.	4E2-3.1
N/A	2.9	Furnish limit-stops (with overrides) on all pullout racks and drawers.	4E2-3.2
N/A	2.10	Provide guide pins on subassemblies for alignment during mounting.	4E2-3.2
Y	2.11	Locate components so there is sufficient space to use test probes, soldering irons, and similar tools without difficulty.	4E2-3.3
N/A	2.12	Do not use resistors, capacitors, and wiring that interfere with tube replacement.	4E2-3.3
N/A	2.13	Locate tubes so they can be replaced without removing assemblies and subassemblies.	4E2-3.3
N/A	2.14	Locate cables so they cannot be abraded, chafed, or used for handholds.	4E2-3.4
N/A	2.15	Locate cables so they are not bent and unbent sharply when they are connected and disconnected.	4E2-3.4
N/A	2.16	Route cables so they cannot be pinched by doors, lids, or covers.	4E2-3.4
N/A	2.17	Provide delicate conductors such as wave guides and high-frequency cables with guards, protective routing, or similar protection.	4E2-3.4
N/A	2.18	Incorporate fail-safe features into equipment designs and installations where the failure or malfunction of the equipment may injure the operator or damage the equipment or adjacent equipment.	Ref 477 799 1253
N/A	2.19	Do not use components containing mercury unless it is essential. If it becomes necessary, design to minimize the probability of damage which would result from mercury spillage.	

3. GENERAL CONSIDERATIONS FOR SYSTEMS

N/A	3.1	Vent lead-acid batteries to areas where ignition is not possible.	3H1-6.6
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APPENDIX D
SPECIFICATION DLP-040776-A
SCR CHIP FOR PULSE APPLICATION

SPECIFICATION DLP-040776-A
SCR CHIP FOR PULSE APPLICATION

1.0 SCOPE

This specification describes a silicon rectifier chip to be used in hybrid circuitry in parallel/series configurations. The chip performance must equal or exceed that of the packaged 2N3873 SCR device.

2.0 APPLICABLE DOCUMENTS

Design and manufacture shall be to best commercial practice, using applicable NEMA or ASA standards.

3.0 REQUIREMENTS

3.1 Operating forward and reverse off state voltage: 600 volts minimum.

3.2 Repetitive Peak Pulse Current (20 Microsecond pulse): 600 Amperes Peak.

3.3 RMS Current Rating: 40 Amperes minimum.

3.4 Typical Pulse Current Rise Time, 10% to 90%: 1 Microsecond.

3.5 Rate of Rise of Off State Voltage: 200 Volts/Microsecond, minimum.

3.6 Recovery Time (Turn Off Time): 40 Microseconds Maximum.

3.7 Operating Junction Temperature: 125⁰C Maximum.

3.8 Construction:

3.8.1 Glass Passivation required.

3.8.2 0.20 inch square chip.

3.8.3 Center Fired Gate.

3.8.4 "Shorted Gate" Design.

3.8.5 Solder Coated Electrodes (95/5 Solder).

4.0 HANDLING AND SHIPPING REQUIREMENTS: To be specified by Vendor.

APPENDIX E

SPECIFICATION DLP 041576A

HYBRID CIRCUIT SUBSTRATE

SPECIFICATION DLP 041576A

HYBRID CIRCUIT SUBSTRATE

- 1.0 Size and Dimensional tolerances to be in accordance with the attached sketch, DLP 041576A.
- 2.0 Both sides of the substrate shall be suitable for metalizing. Surface finish, as fired, to be 15 micro inches minimum, 25 micro inches maximum.
- 3.0 Maximum camber to be 0.006 inches per inch.
- 4.0 Edge Chips: Less than 0.040 inches in at any edge.
- 5.0 Thickness: 0.10 inches ± 0.01 inches is specified; however, if a greater thickness is more economical, the greater thickness may be accepted.
- 6.0 Material:
 - Part 1: Beryllia, with 99.5% minimum B_2O_3 content.
 - Part 2: Alumina, with 99.5% minimum aluminum oxide content.



Figure E-1. Hybrid Circuit Substrate (DLP 041576A)

APPENDIX F
MODULE LAYOUT DRAWINGS

APPENDIX F

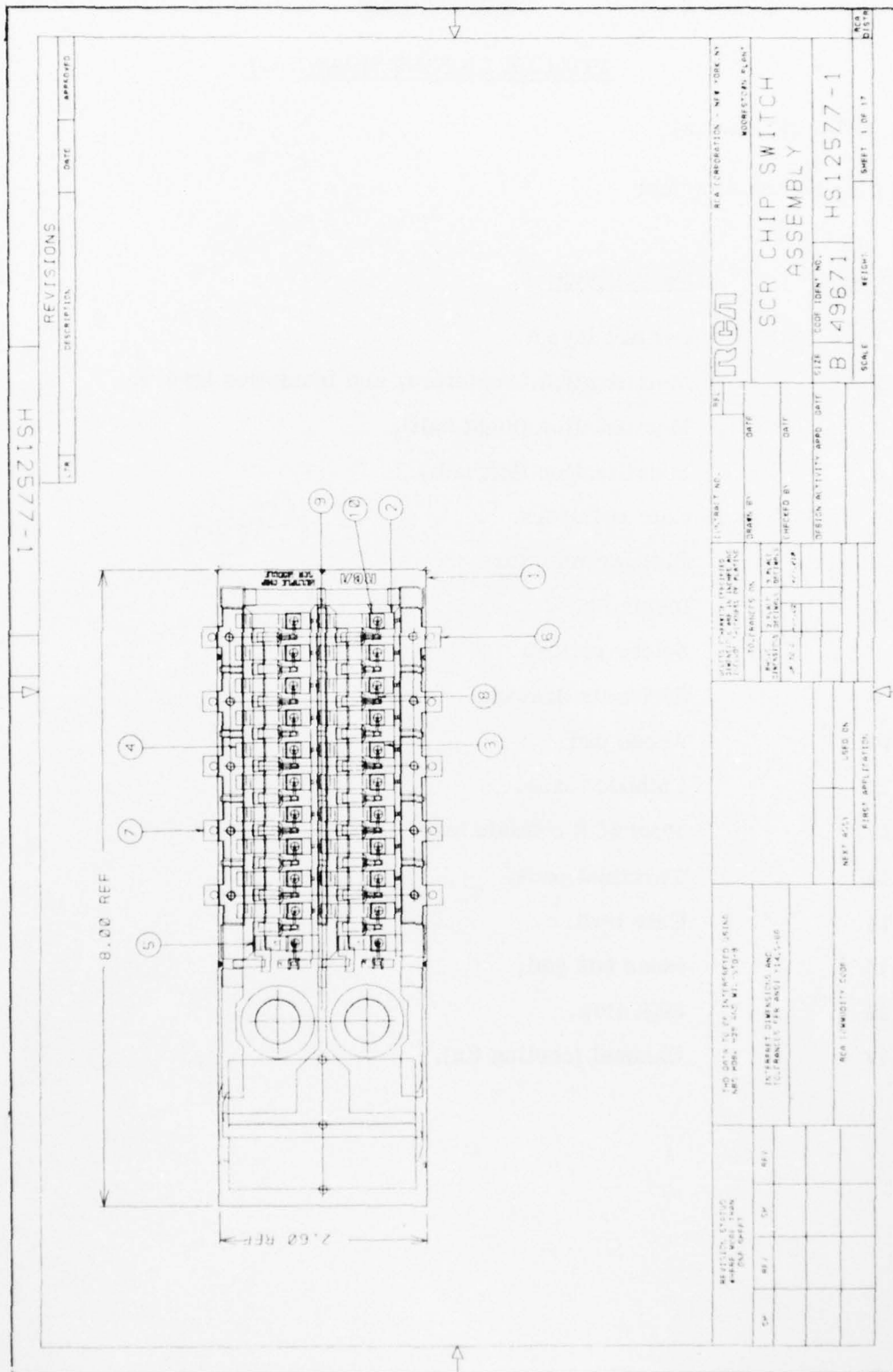
MODULE LAYOUT DRAWINGS

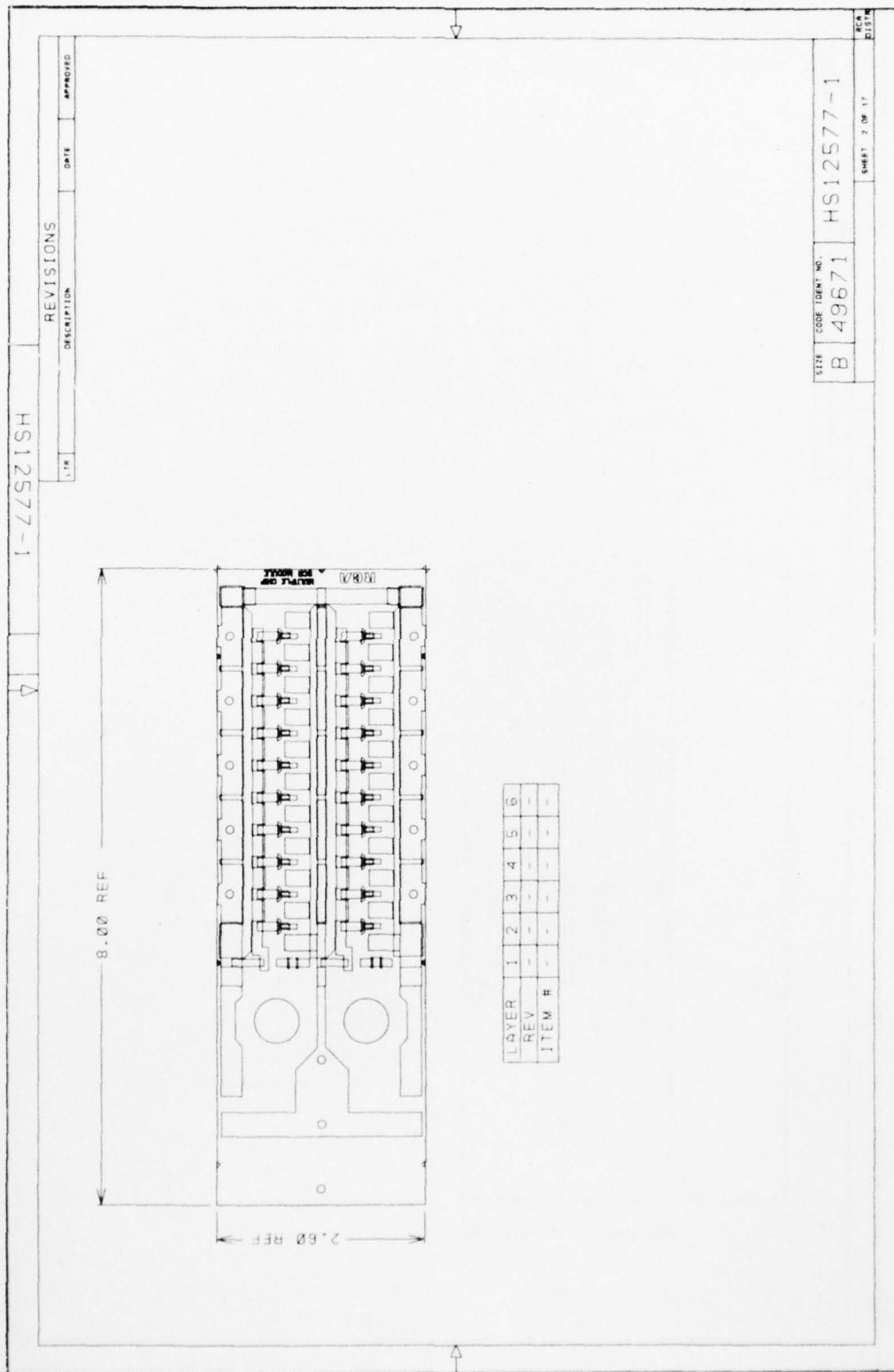
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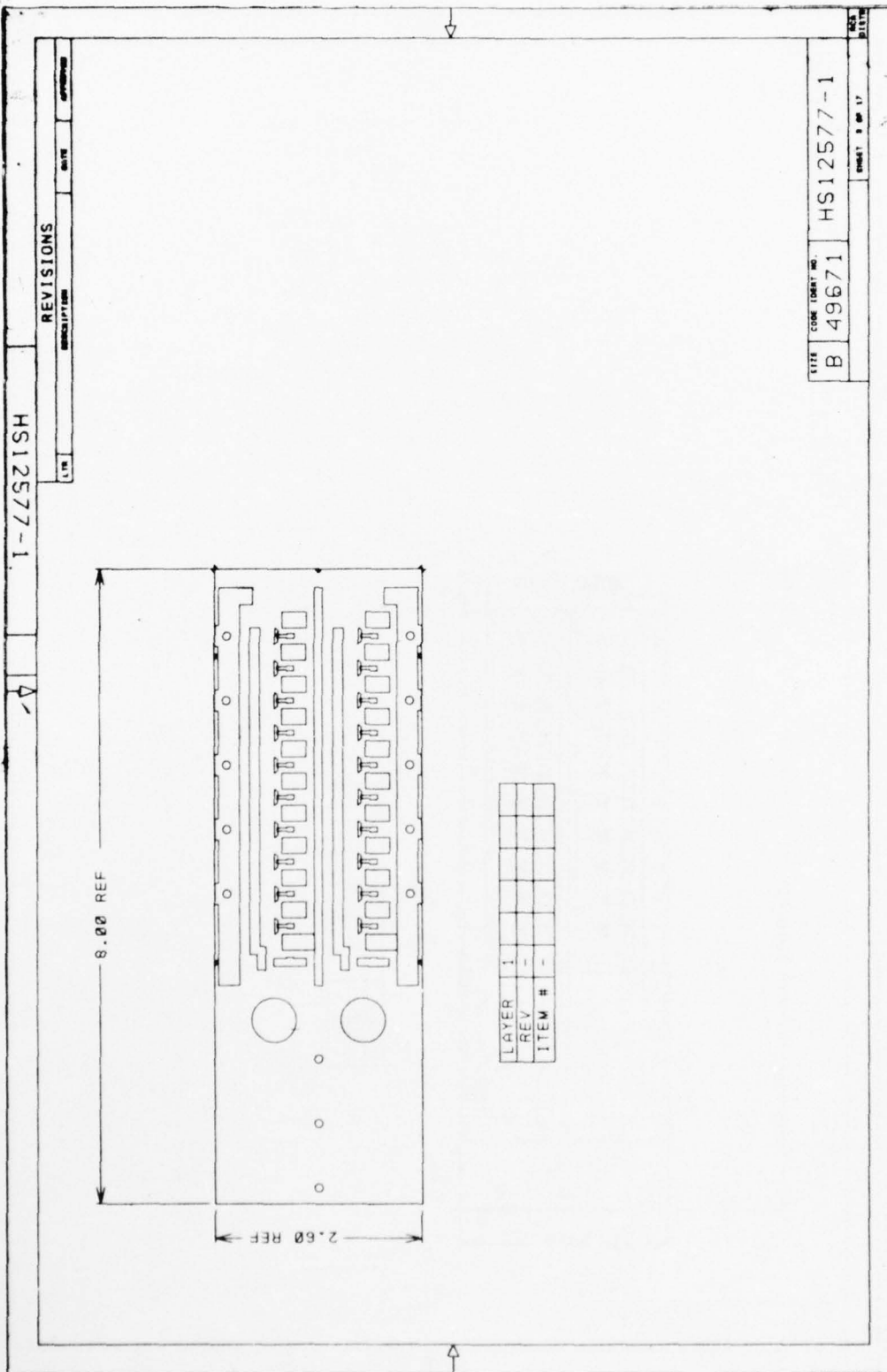
SCR Chip Switch Assembly

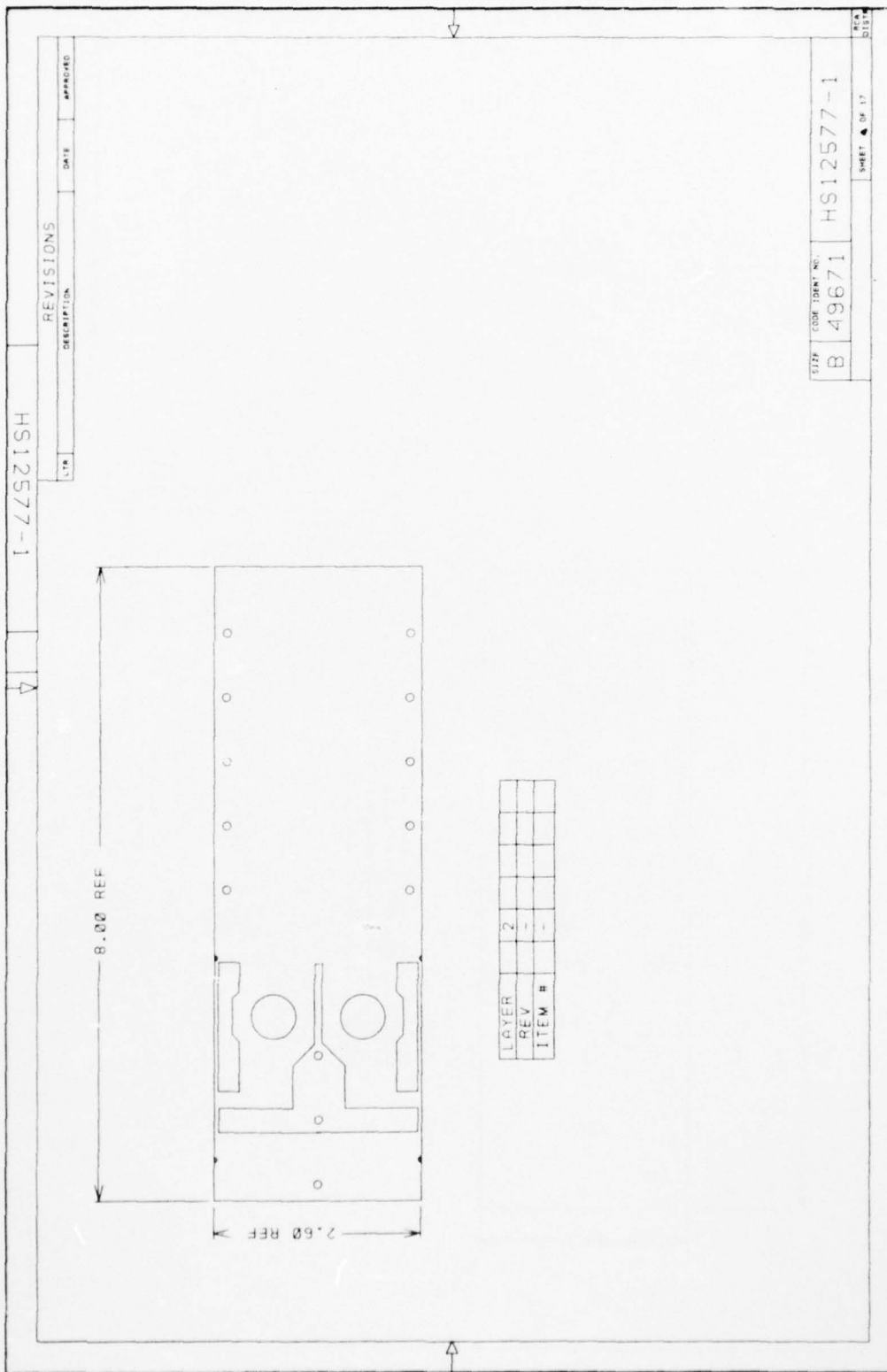
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2	Metallization, resistors, and insulation layers.
3	Metallization (right half).
4	Metallization (left half).
5	Gate resistors.
6	Bleeder resistors
7	Insulation
8	Solder pattern.
9	Substrate drawing.
10	Anode pad.
11	Cathode leads.
12	Pilot SCR cathode lead.
13	Terminal pads.
14	Gate lead.
15	Inner bus pad.
16	SCR chip.
17	Channel (cooling fin).

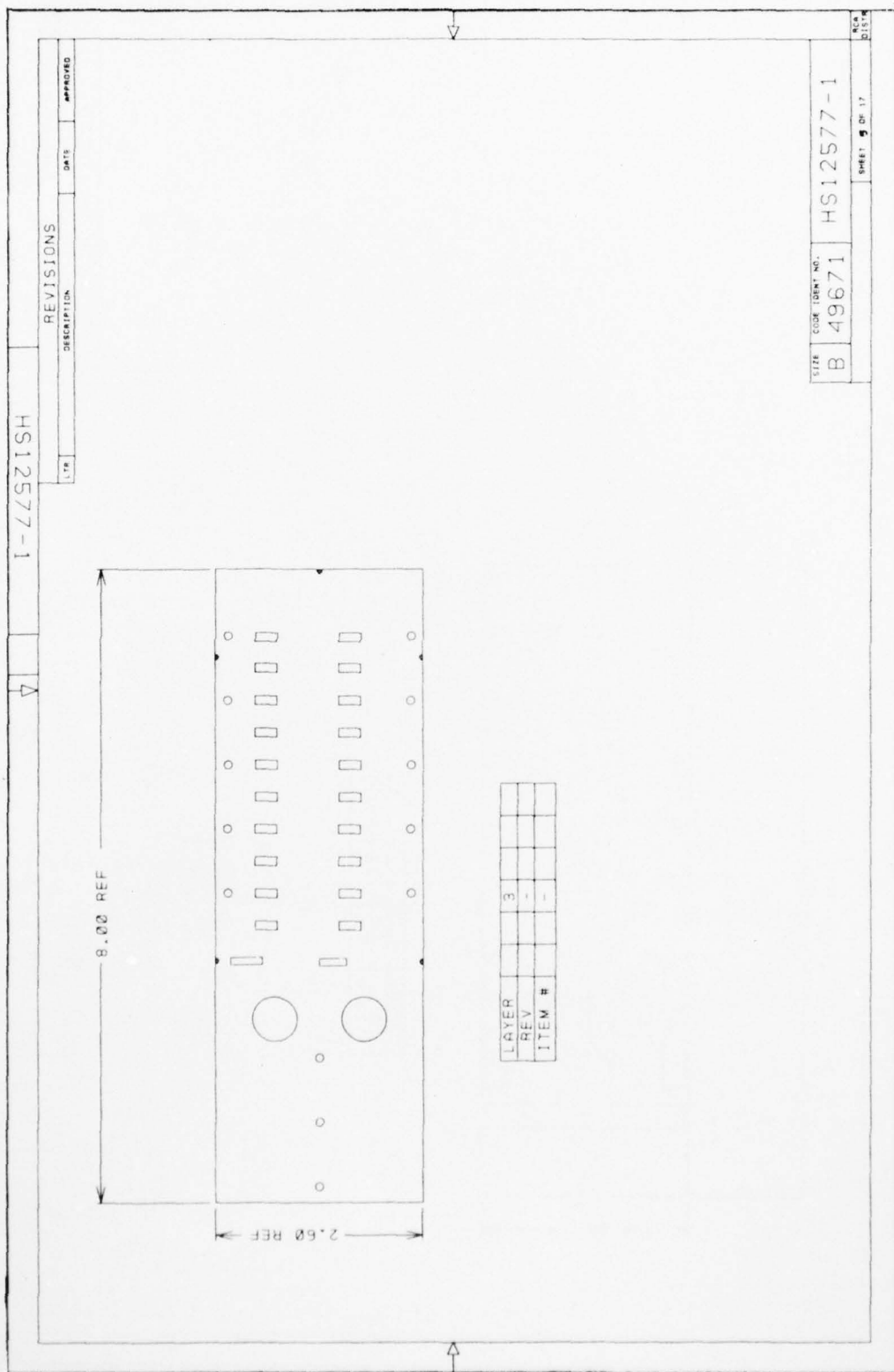
BEST AVAILABLE COPY

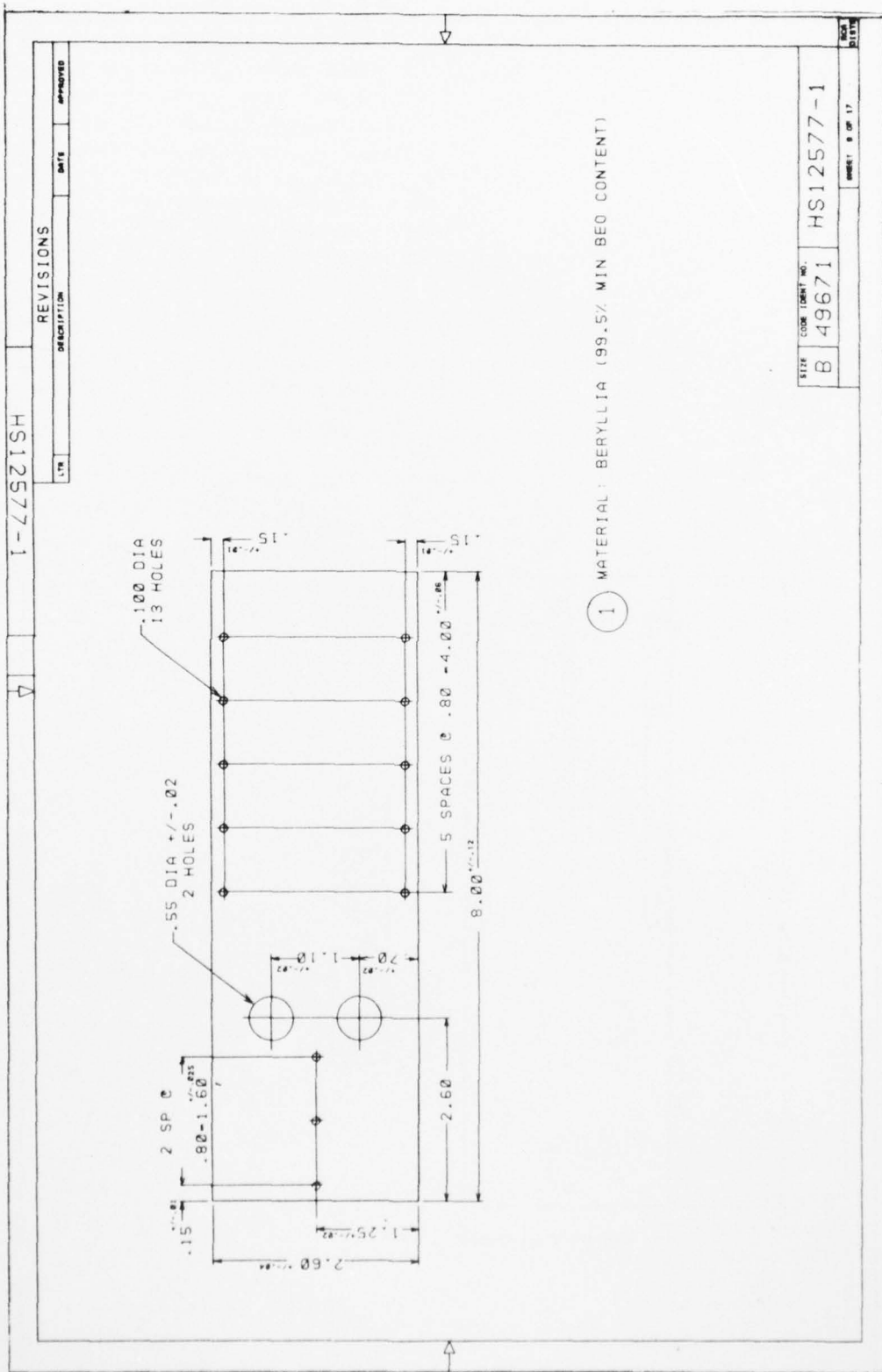




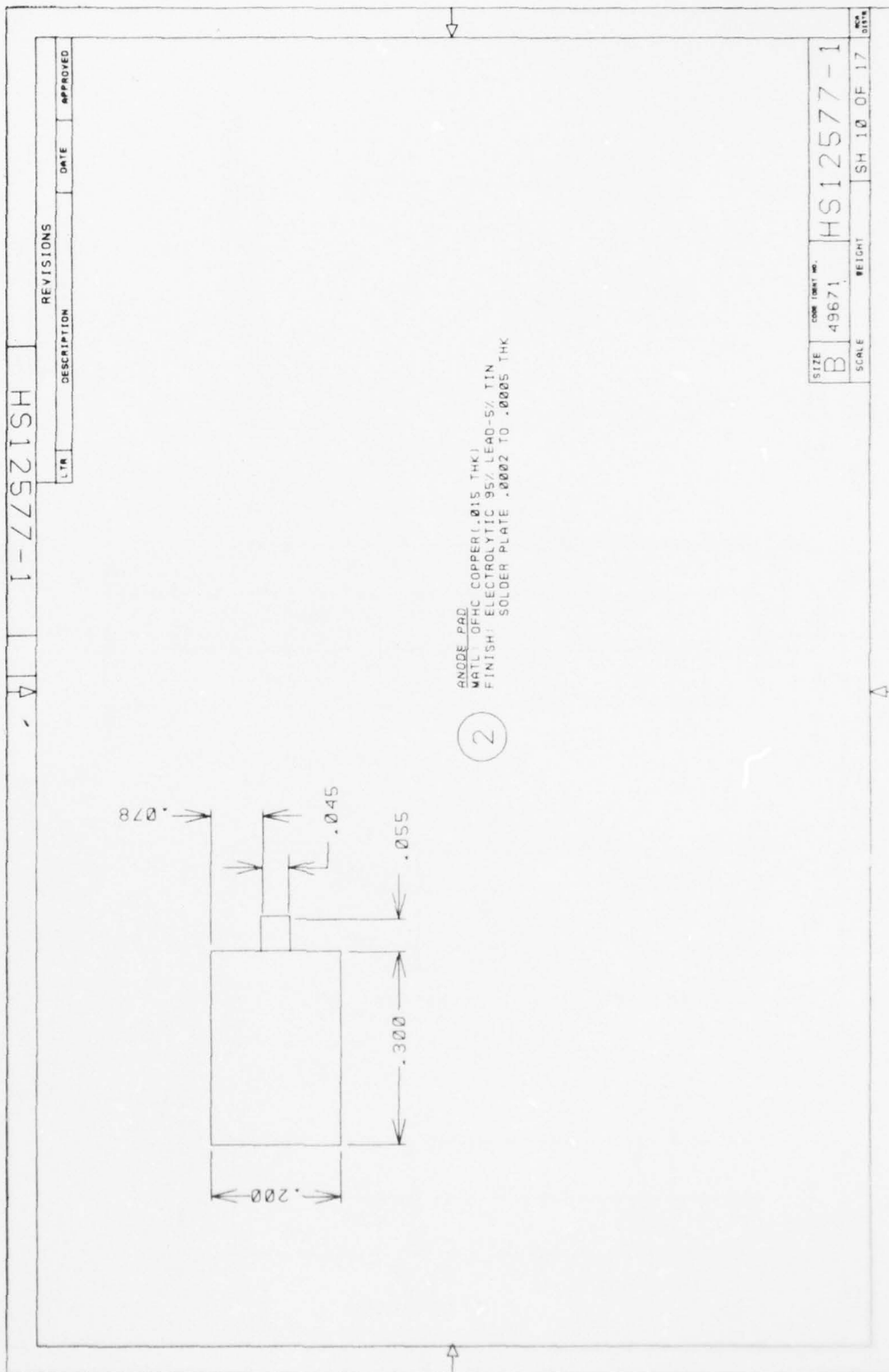








1 MATERIAL: BERYLLIA (99.5% MIN BEO CONTENT)



AD-A044 035

RCA GOVERNMENT SYSTEMS DIV MOORESTOWN N J MISSILE AND--ETC F/G 9/5
MULTIPLE CHIP SCR.(U)

AUG 77 R CASOLARO, D PRUITT

UNCLASSIFIED

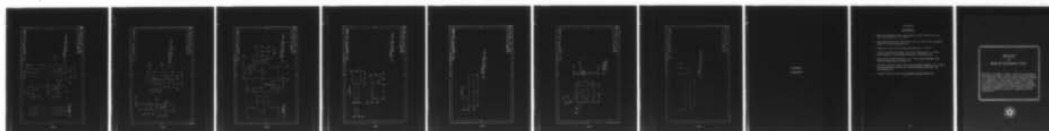
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F30602-76-C-0197

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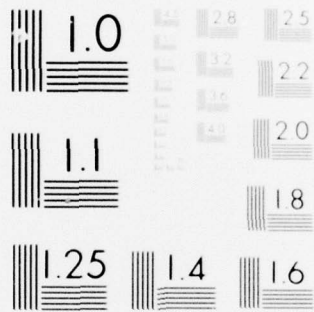
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A044035



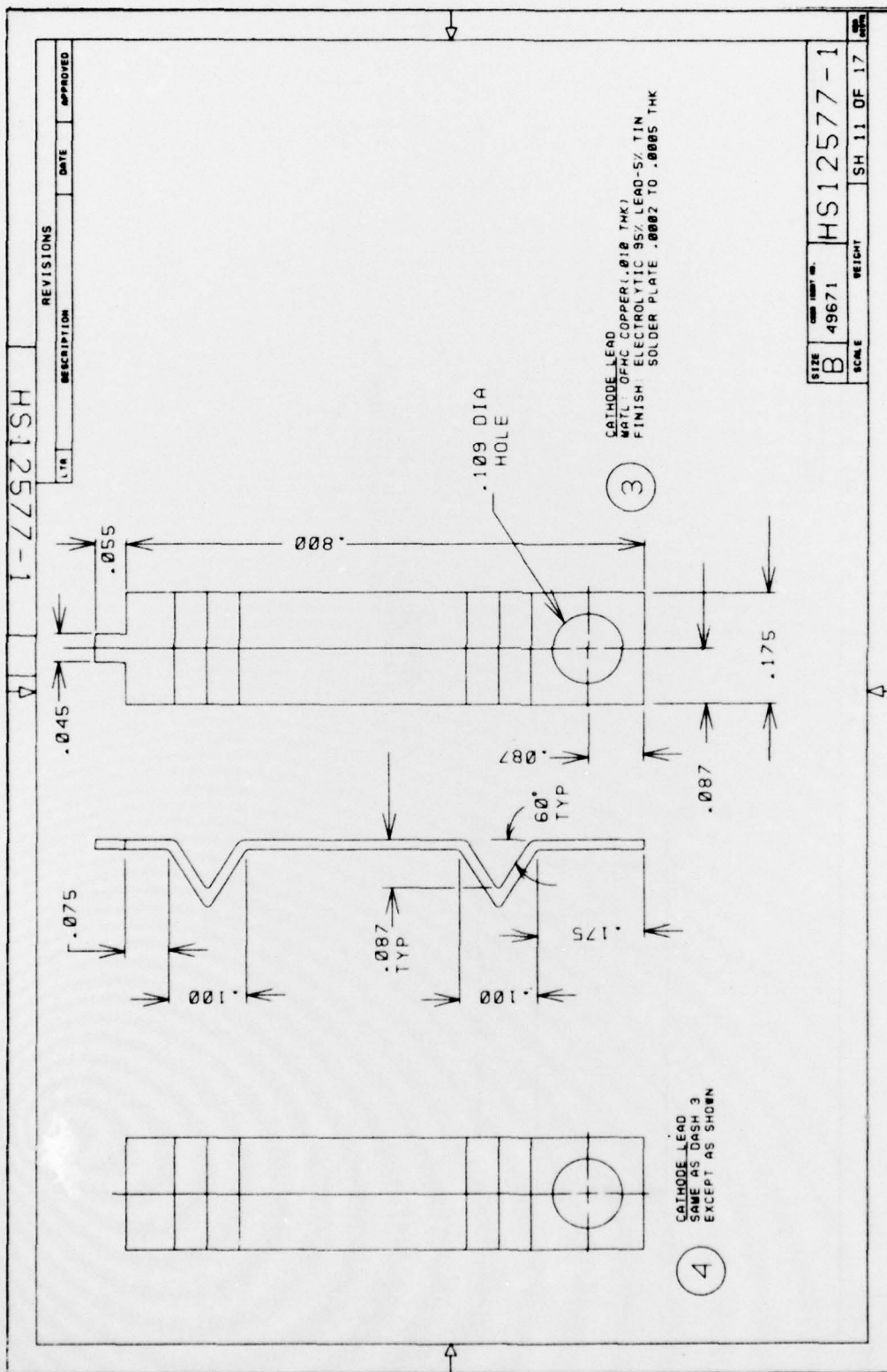
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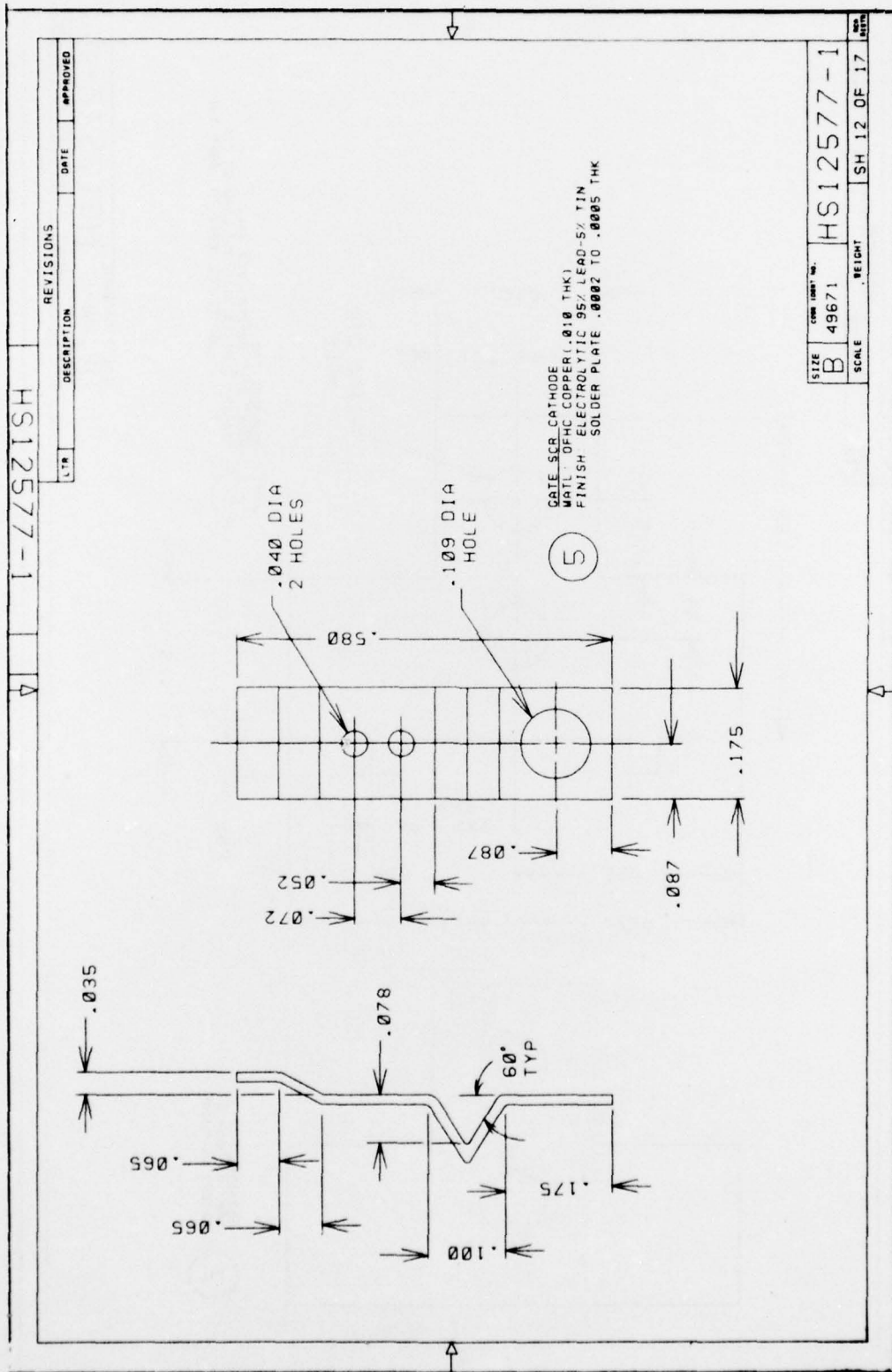
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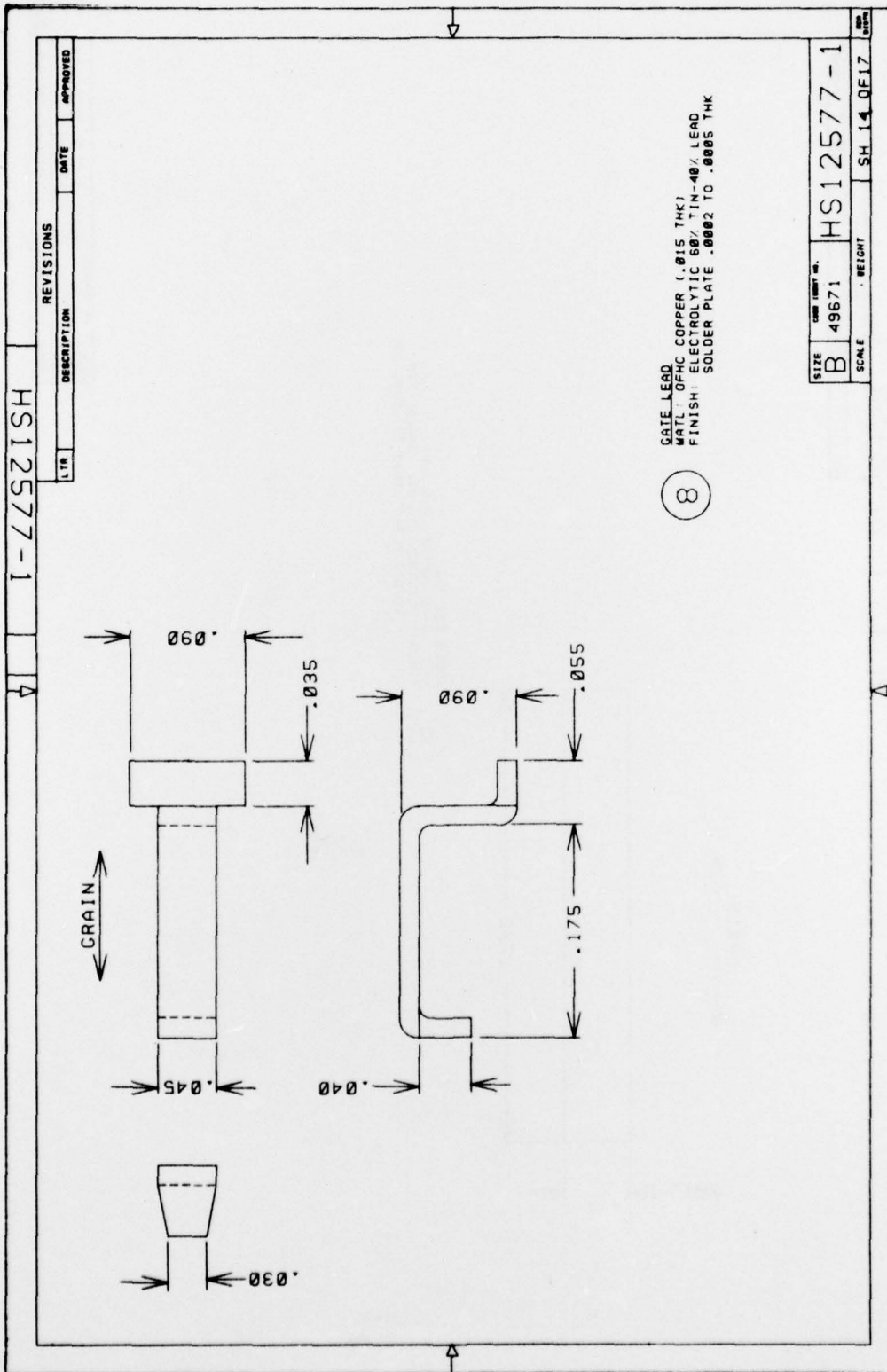
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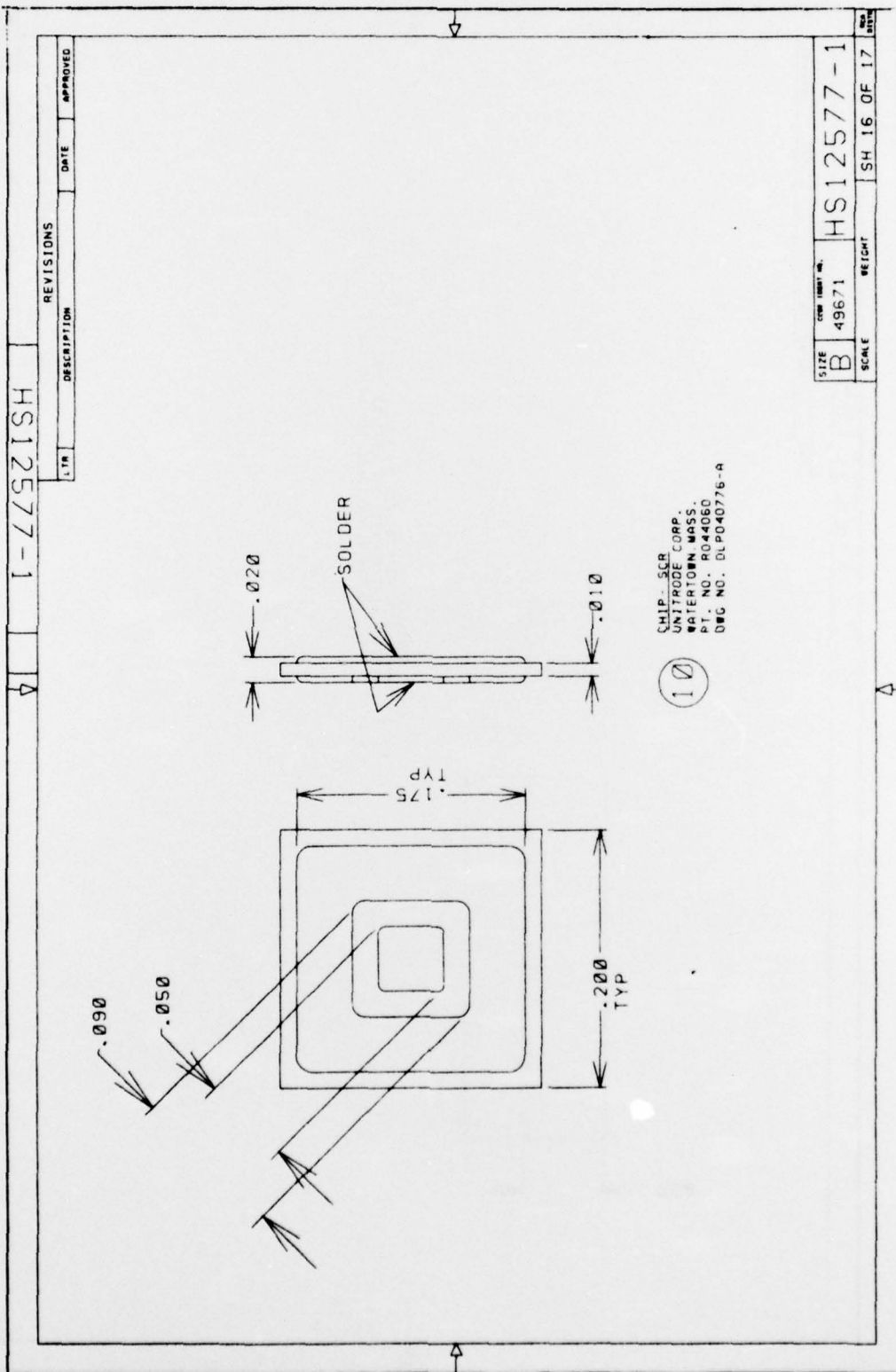


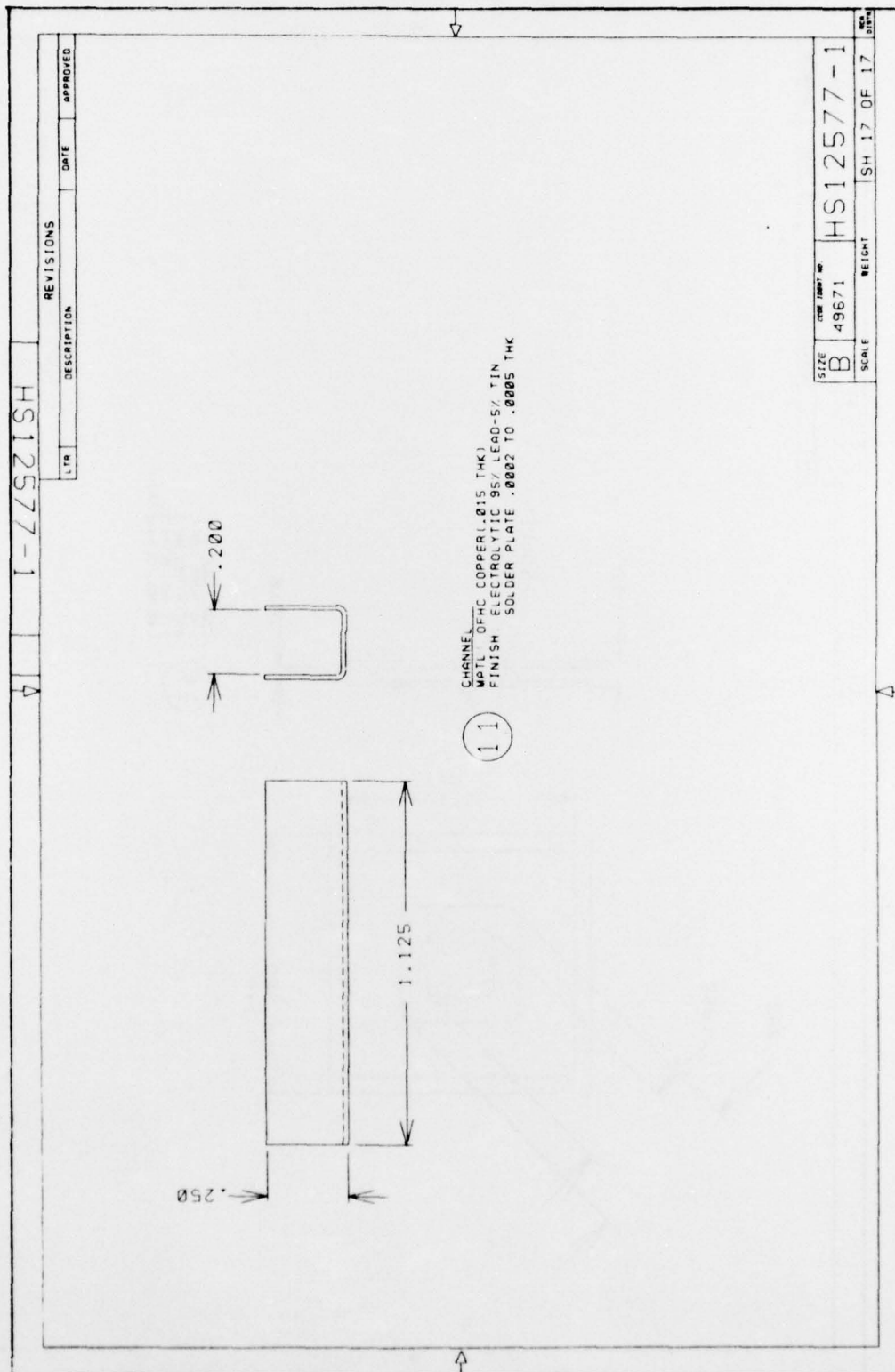
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A











REVISIONS		
DATE	DESCRIPTION	APPROVED

SIZE	QTY	REV	DATE	BY	CHK
B	49671	HS12577-1	SH 17 OF 17		
SCALE	HEIGHT				

APPENDIX G

REFERENCES

APPENDIX G

REFERENCES

1. "High Energy High Duty Pulser" final report on contract F30602-73-C-0151, March 1974, RADC-TR-74-77, (780031).
2. "Multi-Megawatt Solid State Switch" RADC-TR-75-75, final report on contract F30602-74-C-0195, dated March 1975.
3. Supplement to RADC-TR-75-75 dated September 1975, (B007720).
4. "Design Considerations for Super Power Pulse Modulators", D. L. Pruitt, paper presented at 11th Modulator Symposium, 18 September 1973.
5. "Multi-Megawatt Solid State Switch", D. L. Pruitt, paper presented at 12th Modulator Symposium, 4 February 1976.
6. "Thyristor Switches for Super Power Intermittent Duty Operation", D. L. Pruitt, paper presented at the Pulsed Power Systems Workshop, White Oak, MD, 20 September 1976.
7. "Multiple Chip SCR", RCA Proposal 6T0062-A1 dated October 1975.

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